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(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi, Kanagawa-ken (JP)

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See application file for complete search history.

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(57) **ABSTRACT**

The semiconductor device includes a source line, a bit line, a first signal line, a second signal line, a word line, memory cells connected in parallel between the source line and the bit line, a first driver circuit electrically connected to the source line and the bit line, a second driver circuit electrically connected to the first signal line, a third driver circuit electrically connected to the second signal line, and a fourth driver circuit electrically connected to the word line. The memory cell includes a first transistor including a first gate electrode, a first source electrode, and a first drain electrode, a second transistor including a second gate electrode, a second source electrode, and a second drain electrode, and a capacitor. The second transistor includes an oxide semiconductor material.

**33 Claims, 24 Drawing Sheets**
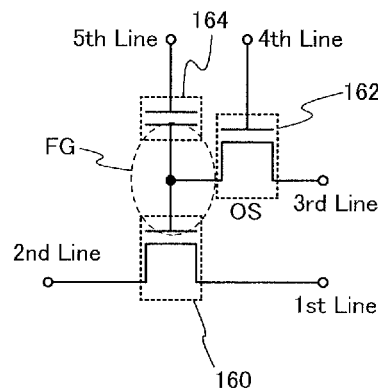
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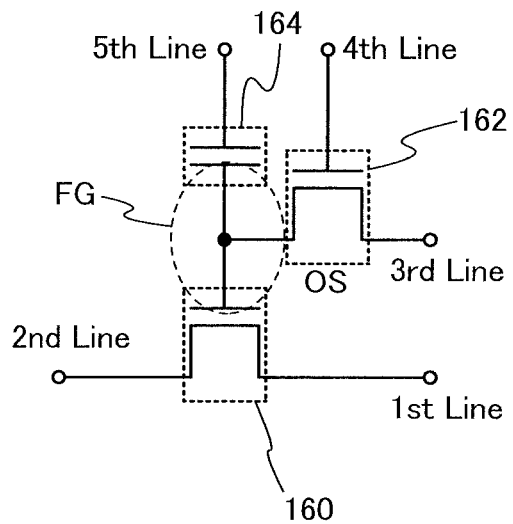
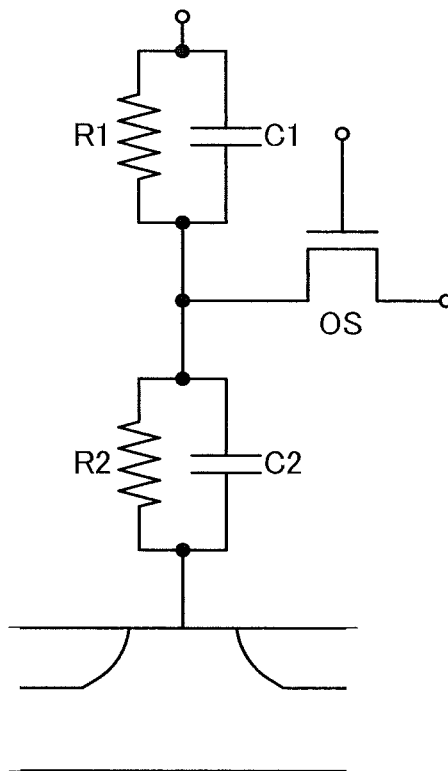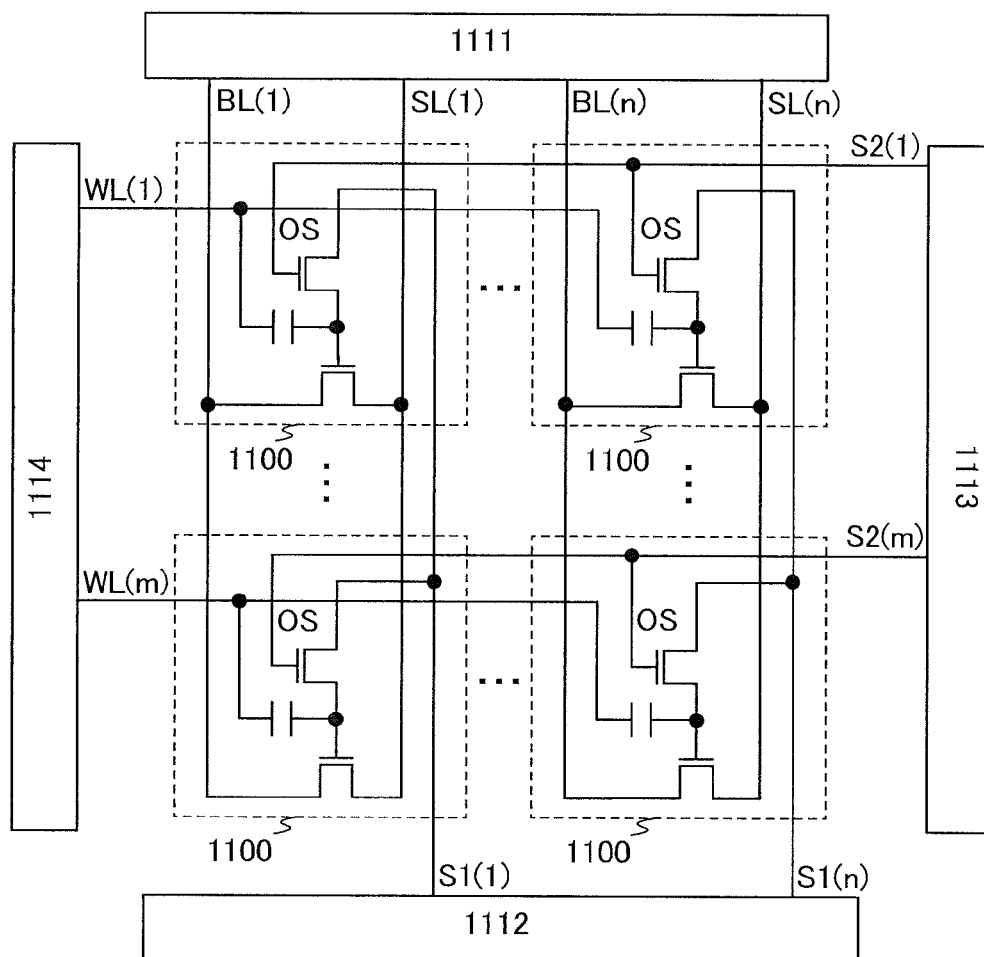* cited by examiner
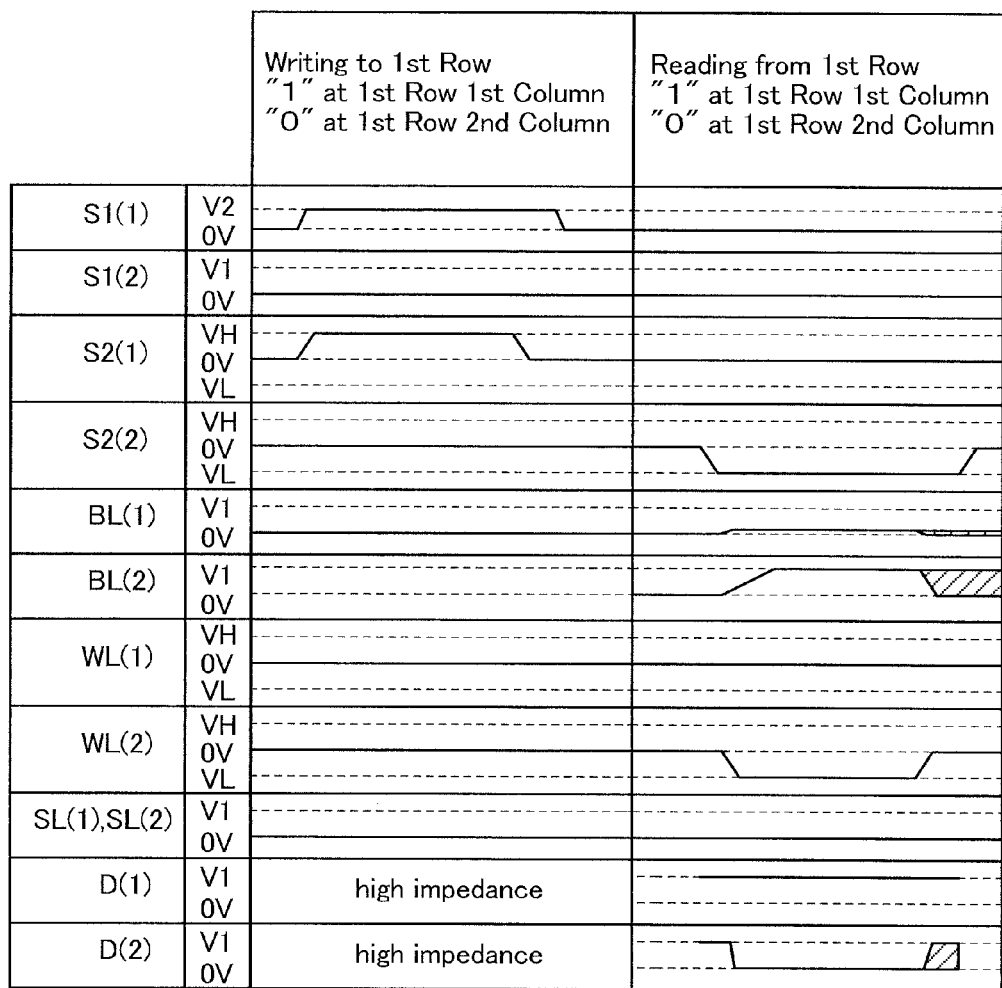
FIG. 1A-1



FIG. 1A-2

FIG. 2

# FIG. 3

| | | Writing to 1st Row<br>"1" at 1st Row 1st Column<br>"0" at 1st Row 2nd Column | Reading from 1st Row<br>"1" at 1st Row 1st Column<br>"0" at 1st Row 2nd Column |
|---|---|---|---|
| S1(1) | V2<br>0V | | |
| S1(2) | V1<br>0V | | |
| S2(1) | VH<br>0V<br>VL | | |
| S2(2) | VH<br>0V<br>VL | | |
| BL(1) | V1<br>0V | | |
| BL(2) | V1<br>0V | | |
| WL(1) | VH<br>0V<br>VL | | |
| WL(2) | VH<br>0V<br>VL | | |
| SL(1),SL(2) | V1<br>0V | | |
| D(1) | V1<br>0V | high impedance | |
| D(2) | V1<br>0V | high impedance | |

FIG. 4

FIG. 5

FIG. 6

# FIG. 7

FIG. 8A

130a  142c  142d  130b  150  148b  142a  144  148a  146  142b

152
150
146

128
126

110
106

A1                           A2  B1                                    B2

124  114         108  118    110      130c    164      100    162
  120    160  116                    108

FIG. 8B

142b  B2
140          148a

162          142a

164          148b
110
             160
A1              A2
142c          142d

FIG. 9A

102

100

A1 A2

FIG. 9B

104 106

A1 A2

FIG. 9C

112 108
110 116
114

A1 A2

FIG. 9D

118

A1 A2

FIG. 9E

122

120

A1 A2

FIG. 9F

124

A1 A2

FIG. 9G

128

126

A1 A2

FIG. 9H

130a 130b

170

A1 A2

FIG. 10A

142a 128 142b

B1 B2

FIG. 10B

144

B1 B2

FIG. 10C

146

B1 B2

FIG. 10D

148b 148a

B1 B2

FIG. 10E

150 152

B1 164 162 B2
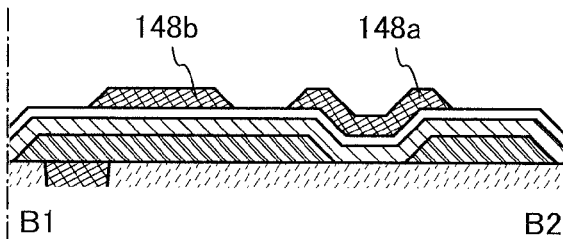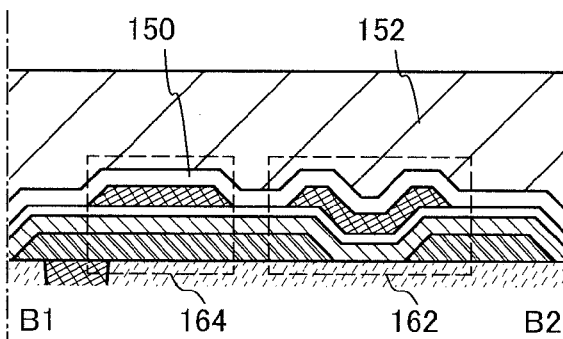
FIG. 11A



FIG. 11B

FIG. 12A

130a          130b
128
126
110
106

A3                    A4  B3                                        B4

124    114        108    118    110                    164    100    162
120    160    116            108

FIG. 12B

142c  142d                        142a                        142b

A3                A4  B3                                        B4

FIG. 12C

144                146

A3                A4  B3                                        B4

FIG. 12D

148b    150    152                                148a

A3                A4  B3                                        B4
164                162

FIG. 13A

144  148b  156                    156    142a    144      126
142a | 146 | 164 /      152  154  150 \148b    143a   | 148a | 146  143b

C1                              C2 | D1                                    D2

110        108              124 / 110    116      164  \ 100    125
     160  116  106          120    160        108      128    162  142b

FIG. 13B

162 — 142b                              106

148a

142a

148b        C1                C2

164
160

124              D1

FIG. 14A

142a     128     126

C1    C2 D1                                    D2

110     108          124  110    116        100   125
   160 116 106      120    160    108    142a     142b

FIG. 14B

143a          143b

C1          C2 D1                              D2

FIG. 14C

146          144

C1          C2 D1                              D2

FIG. 14D

148b          148b          148a

C1          C2 D1                              D2

FIG. 15A



C1　　　　　　　C2 D1　　　　　　　　　　　　　D2

FIG. 15B



C1　　　　　　　C2 D1　　　　　　　　　　　　　D2

FIG. 15C



C1　　　　　　　C2 D1　　　　　　　　　　　　　D2

FIG. 16A

FIG. 16D

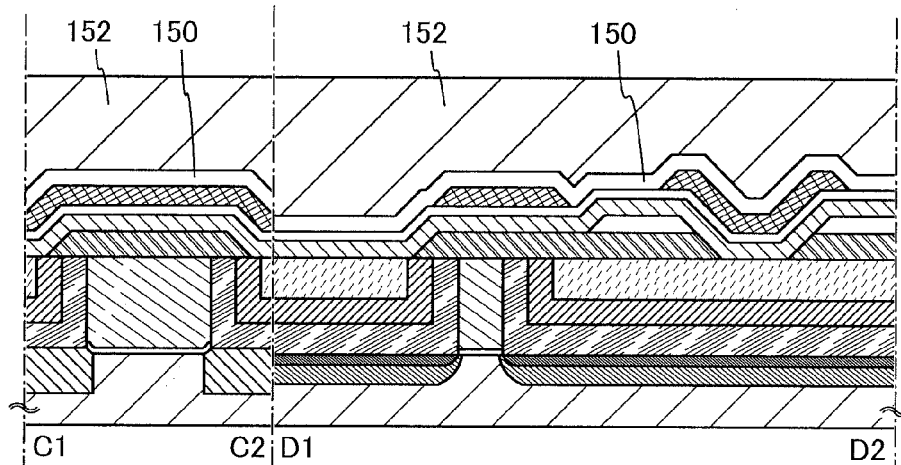FIG. 16B

FIG. 16E

FIG. 16C

FIG. 16F

FIG. 17



Writing at a High State

Writing at a Low State

1.0E-02
1.0E-04
1.0E-06
Id[A] 1.0E-08
1.0E-10
1.0E-12
1.0E-14

-7  -6  -5  -4  -3  -2  -1  0  1  2  3  4  5

Vcg[V]

——— 1st Writing at a High State (Vds = 1 V)
············ $1 \times 10^9$th Writing at a High State (Vds = 1 V)
——— 1st Wriging at a Low State (Vds = 1 V)
············ $1 \times 10^9$th Writing at a High State (Vds = 1 V)

FIG. 18



ID-VG characteristics

# FIG. 19

FIG. 20

| | Initialization Period | Measurement Period |
|---|---|---|
| V1 | VDD | |
| V2 | | VSS |
| Vext_b1 | | |
| Vext_b2 | | |
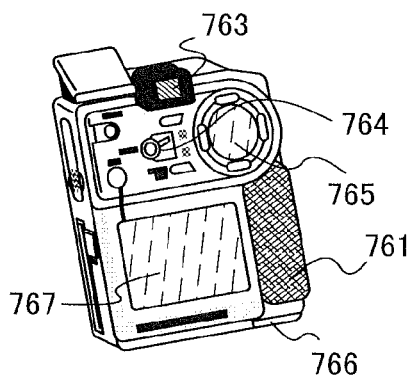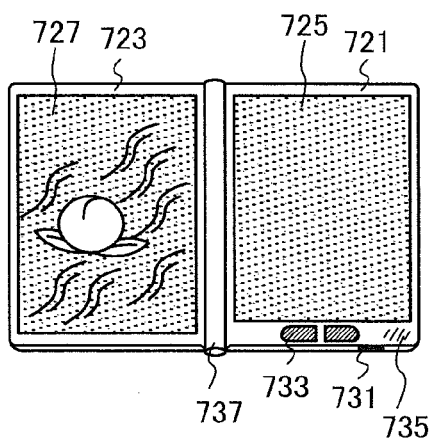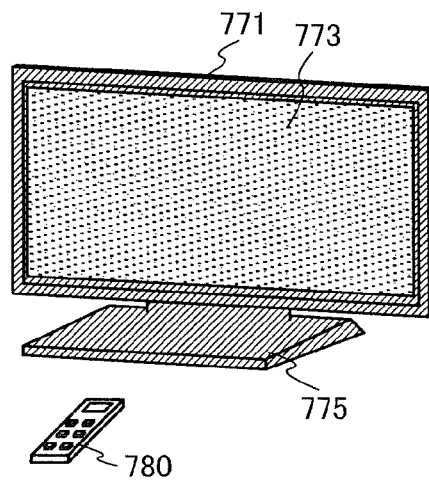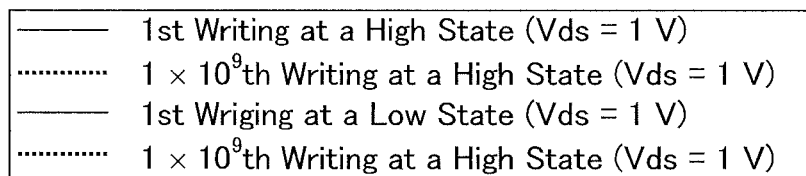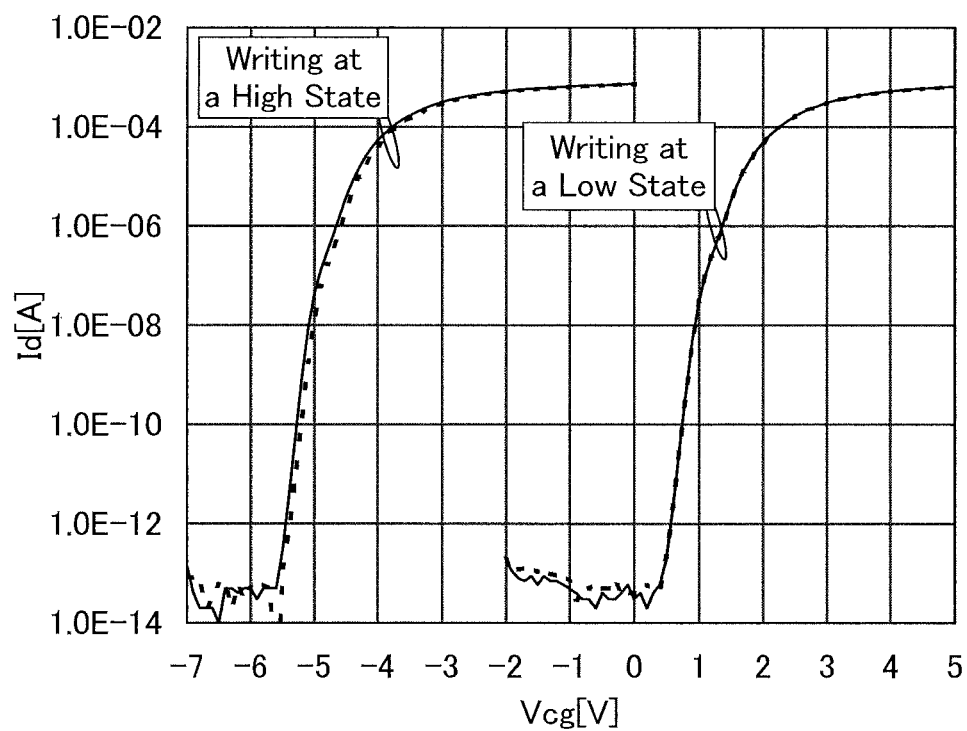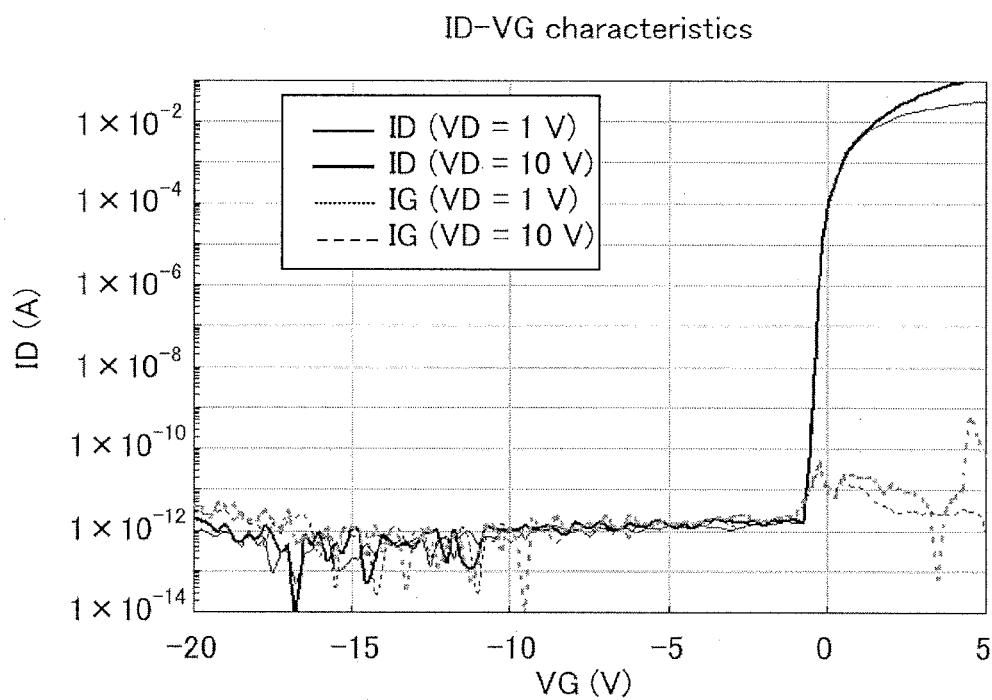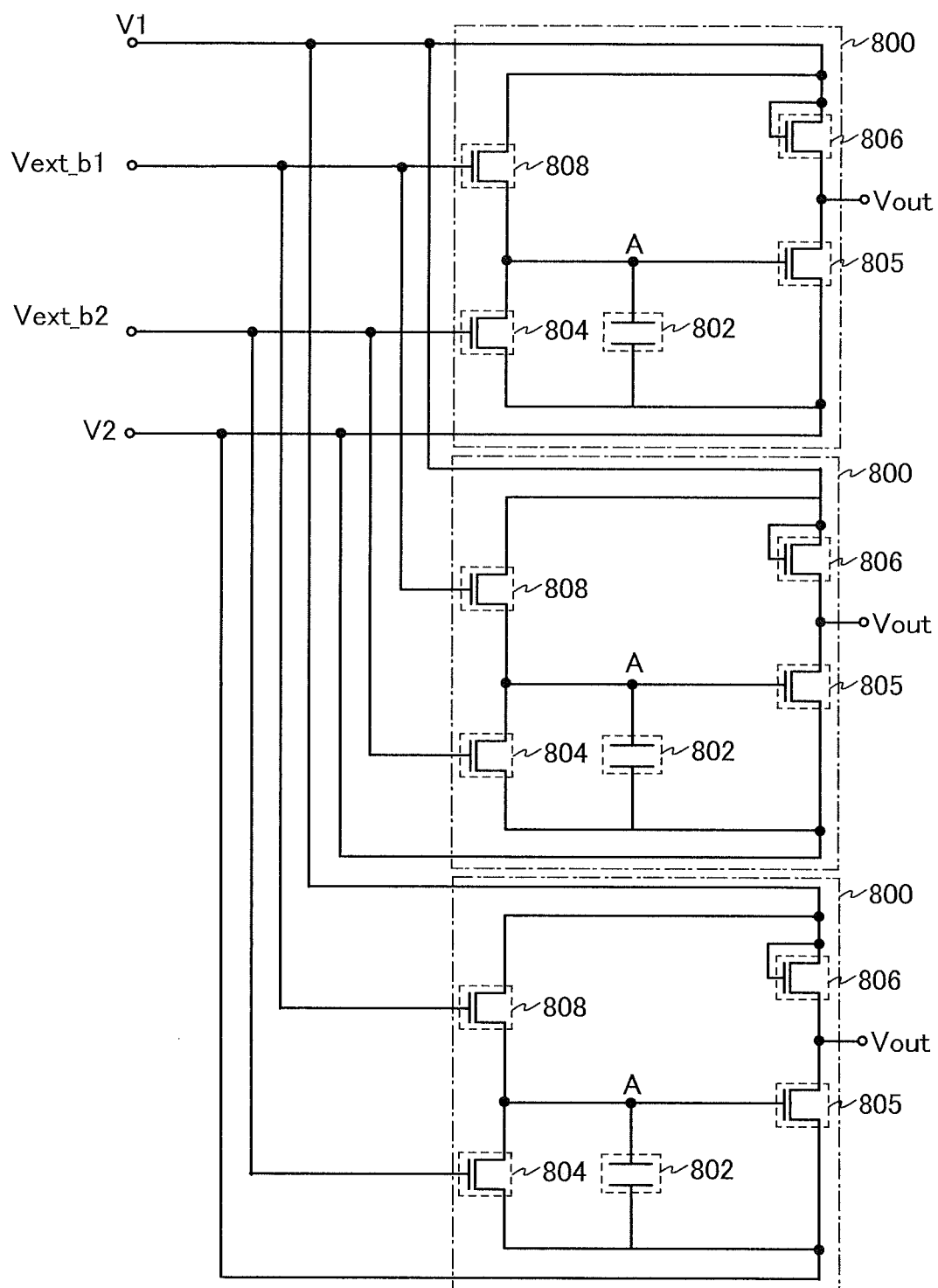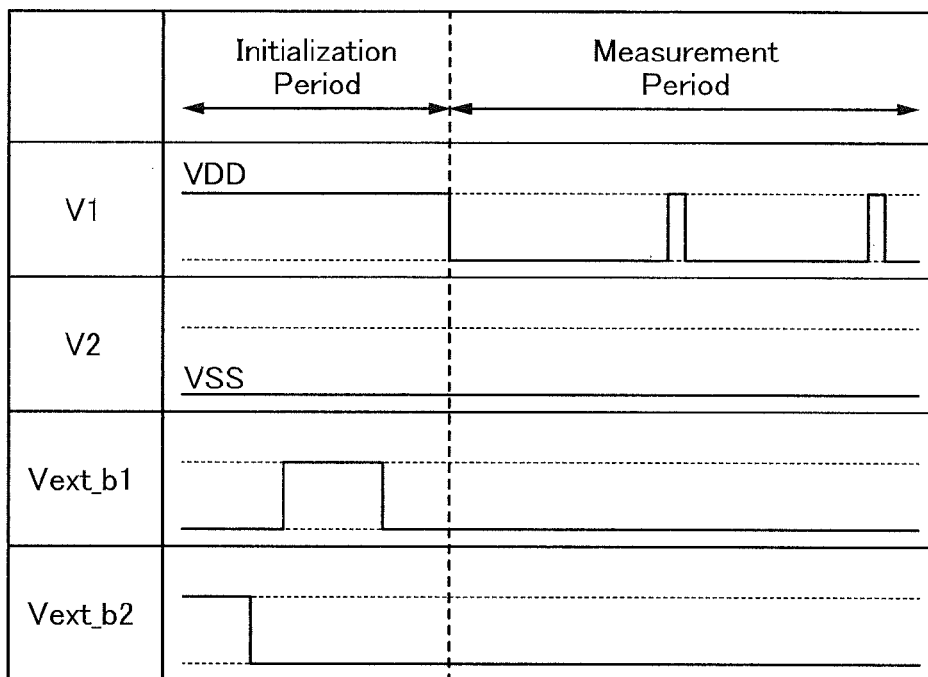
FIG. 21
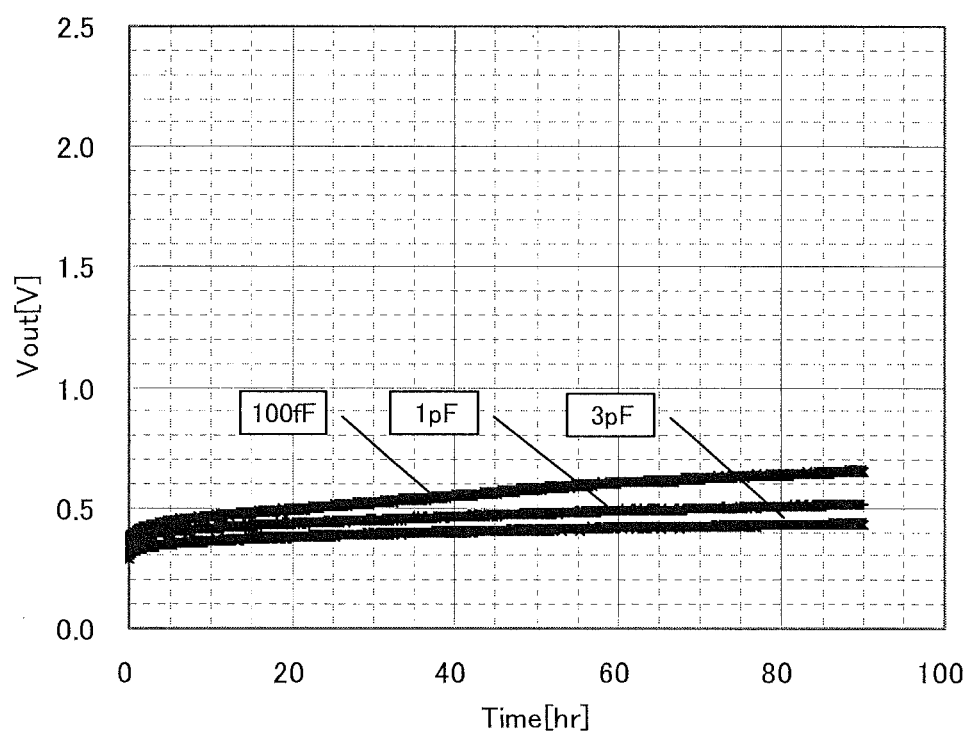
FIG. 22

FIG. 23A

FIG. 23B

## FIG. 24A

144

128
126
110
106

E1                    E2 F1                    F2

124 / 114 /    \ 108 \118 | 110              100
  120   160 116              108

## FIG. 24B

142c  142d              142a                    142b

E1                    E2 F1                    F2

## FIG. 24C

148b          148a          146

E1                    E2 F1                    F2

## FIG. 24D

165    150  152    163

E1                    E2 F1                    F2
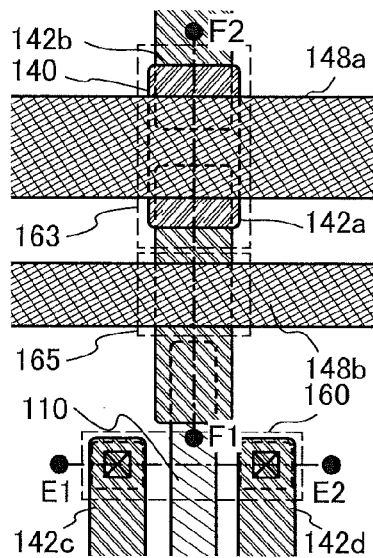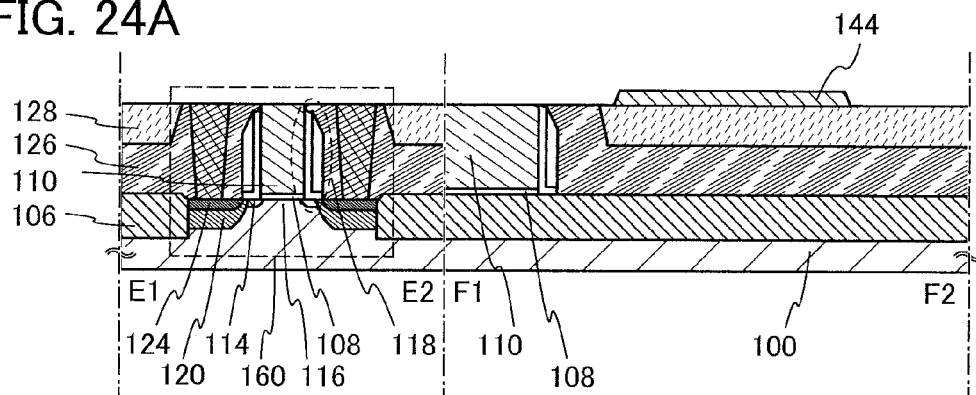
# SEMICONDUCTOR DEVICE

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 12/979,039, filed Dec. 27, 2010, now allowed, which claims the benefit of foreign priority applications filed in Japan as Serial No. 2009-298891 on Dec. 28, 2009, Serial No. 2010-007488 on Jan. 15, 2010 and Serial No. 2010-160954 on Jul. 15, 2010, all of which are incorporated by reference.

## TECHNICAL FIELD

The invention disclosed herein relates to a semiconductor device employing a semiconductor element and a manufacturing method thereof.

## BACKGROUND ART

Storage devices employing semiconductor elements are roughly classified into two categories: a volatile storage device that loses stored data when power supply stops, and a nonvolatile storage device that retains stored data even when power is not supplied.

A typical example of a volatile storage device is a dynamic random access memory (DRAM). A DRAM stores data in such a manner that a transistor included in a memory element is selected and electric charge is stored in a capacitor.

When data is read from a DRAM, electric charge in a capacitor is lost according to the above-described principle; thus, another writing operation is necessary whenever data is read out. Moreover, a transistor included in a memory element has leakage current (off-state current) or the like between a source and a drain in an off state and electric charge flows into or out of a capacitor even if the transistor is not selected, whereby a data (information) holding period is short. For that reason, another writing operation (refresh operation) is necessary at predetermined intervals, and it is difficult to sufficiently reduce power consumption. Furthermore, since stored data is lost when power supply stops, an additional storage device utilizing a magnetic material or an optical material is needed in order to store the data for a long time.

Another example of a volatile storage device is a static random access memory (SRAM). An SRAM retains stored data by using a circuit such as a flip-flop and thus does not need refresh operation. This means that an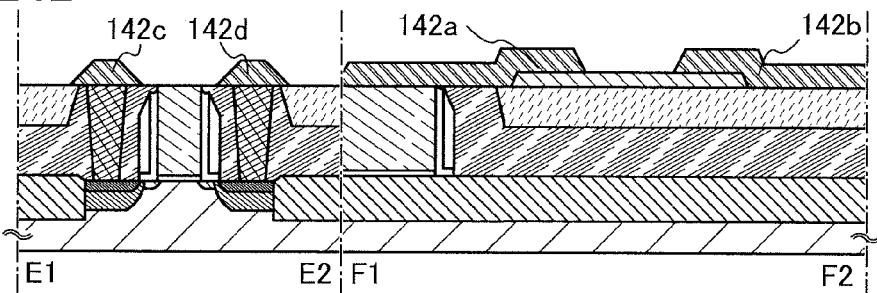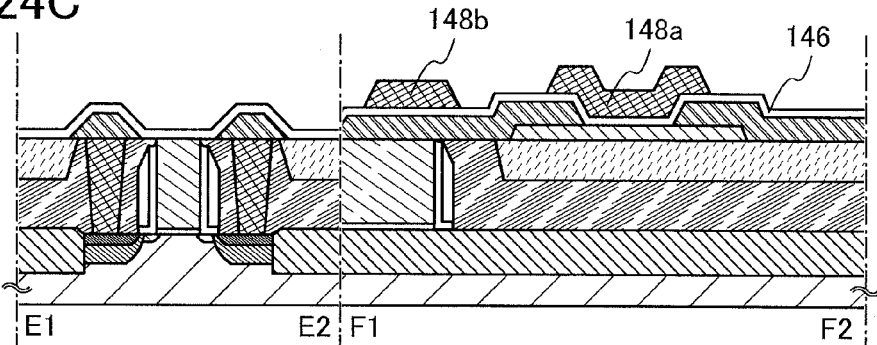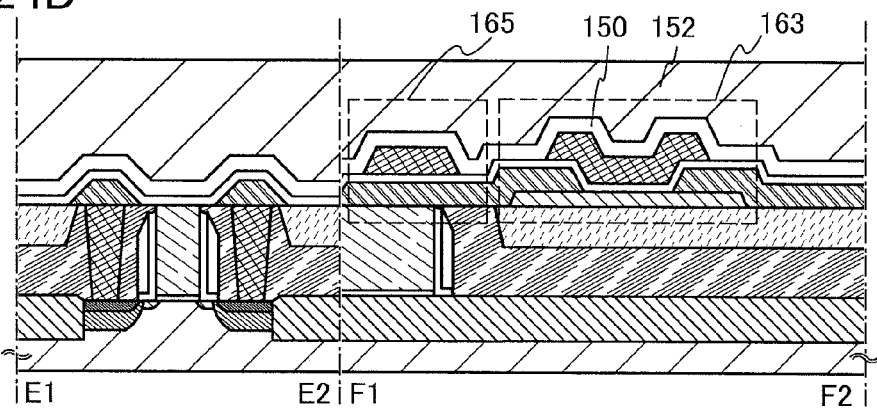 SRAM has an advantage over a DRAM. However, cost per storage capacity is increased because a circuit such as a flip-flop is used. Moreover, as in a DRAM, stored data in an SRAM is lost when power supply stops.

A typical example of a nonvolatile storage device is a flash memory. A flash memory includes a floating gate between a gate electrode and a channel formation region in a transistor and stores data by holding electric charge in the floating gate. Therefore, a flash memory has advantages in that the data holding time is extremely long (almost permanent) and refresh operation which is necessary in a volatile storage device is not needed (e.g., see Patent Document 1).

However, a gate insulating layer included in a memory element deteriorates owing to tunneling current generated in writing, so that the memory element stops its function after a predetermined number of writing operations. In order to reduce adverse effects of this problem, a method in which the number of writing operations for memory elements is equalized is employed, for example. However, a complicated

peripheral circuit is needed to realize this method. Even when such a method is employed, the fundamental problem of lifetime is not solved. In other words, a flash memory is not suitable for applications in which data is frequently rewritten.

In addition, high voltage is necessary for holding electric charge in the floating gate or removing the electric charge, and a circuit for supplying high voltage is required. Further, it takes a relatively long time to hold or remove electric charge, and it is not easy to perform writing and erasing at higher speed.

### REFERENCE

#### Patent Document

[Patent Document 1] Japanese Published Patent Application No. S57-105889

## DISCLOSURE OF INVENTION

In view of the foregoing problems, an object of an embodiment of the invention disclosed herein is to provide a semiconductor device with a novel structure in which stored data can be retained even when power is not supplied, and does not have a limitation on the number of times of writing.

In the disclosed invention, a semiconductor device is formed using a purified oxide semiconductor. The transistor formed using a purified oxide semiconductor has extremely small leakage current, so that data can be stored for a long time.

An embodiment of the disclosed invention is a semiconductor device including a source line, a bit line, a first signal line, a second signal line, a word line, memory cells connected in parallel between the source line and the bit line, a first driver circuit electrically connected to the source line and the bit line, a second driver circuit electrically connected to the first signal line, a third driver circuit electrically connected to the second signal line, and a fourth driver circuit electrically connected to the word line. Each of the memory cells includes a first transistor including a first gate electrode, a first source electrode, and a first drain electrode; a second transistor including a second gate electrode, a second source electrode, and a second drain electrode; and a capacitor. The first transistor includes a semiconductor material other than an oxide semiconductor. The second transistor includes an oxide semiconductor material. The first gate electrode, one of the second source electrode and the second drain electrode, and one electrode of the capacitor are electrically connected to one another. The source line and the first source electrode are electrically connected to each other. The bit line and the first drain electrode are electrically connected to each other. The first signal line and the other of the second source electrode and the second drain electrode are electrically connected to each other. The second signal line and the second gate electrode are electrically connected to each other. The word line and the other electrode of the capacitor are electrically connected to each other.

Further, in the above, the first transistor can have a structure in which a first channel formation region formed using a semiconductor material other than an oxide semiconductor, impurity regions provided with the first channel formation region sandwiched therebetween, a first gate insulating layer over the first channel formation region, the first gate electrode over the first gate insulating layer, and the first source electrode and the first drain electrode which are electrically connected to the impurity regions are included.

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Further, in the above, the second transistor can have a structure in which the second source electrode and the second drain electrode which are provided above the first transistor, a second channel formation region which includes an oxide semiconductor material and is electrically connected to the second source electrode and the second drain electrode, a second gate insulating layer over the second channel formation region, and a second gate electrode over the second gate insulating layer are included.

In the above, the capacitor can include the second source electrode or the second drain electrode, the second gate insulating layer, and an electrode for the capacitor over the second gate insulating layer.

Note that although the transistor is formed using an oxide semiconductor material in the above, the disclosed invention is not limited to this. A material which can realize the off-current characteristics equivalent to those of the oxide semiconductor material, such as a wide gap material like silicon carbide (more specifically, a semiconductor material with an energy gap Eg of greater than 3 eV) may be used.

Note that in this specification and the like, the term such as "over" or "below" does not necessarily mean that a component is placed "directly on" or "directly under" another component. For example, the expression "a gate electrode over a gate insulating layer" can mean the case where there is an additional component between the gate insulating layer and the gate electrode. Moreover, the terms such as "over" and "below" are only used for convenience of description and can include the case where the relation of components is reversed, unless otherwise specified.

In addition, in this specification and the like, the term such as "electrode" or "wiring" does not limit a function of a component. For example, an "electrode" is sometimes used as part of a "wiring", and vice versa. Furthermore, the term "electrode" or "wiring" can include the case where a plurality of "electrodes" or "wirings" is formed in an integrated manner.

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flow is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be replaced with each other in this specification.

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an object having any electric function. There is no particular limitation on an object having any electric function as long as electric signals can be transmitted and received between components that are connected through the object.

Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

Since the off-state current of a transistor including an oxide semiconductor is extremely small, stored data can be retained for an extremely long time by using the transistor including an oxide semiconductor. In other words, power consumption can be sufficiently reduced because refresh operation becomes unnecessary or the frequency of refresh operation can be extremely low. Moreover, stored data can be retained for a long time even when power is not supplied.

Further, in a semiconductor device according to the disclosed invention, high voltage is not needed to write data, and deterioration of the element does not become a problem. For example, unlike a conventional nonvolatile memory, it is not necessary to inject and extract electrons into and from a

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floating gate, so that a problem such as deterioration of a gate insulating layer does not occur. That is, the semiconductor device according to the disclosed invention has no limitation on the number of times of rewriting, which is a problem of a conventional nonvolatile memory, and reliability thereof is drastically improved. Further, writing of data is performed depending on an on state and an off state of the transistor, so that high-speed operation can be easily realized. Additionally, there is an advantage that operation for erasing data is not needed.

Since a transistor including a material other than an oxide semiconductor can operate at sufficiently high speed, a semiconductor device can perform operation (e.g., reading data) at sufficiently high speed in combination of a transistor including an oxide semiconductor. Further, a transistor including a material other than an oxide semiconductor can favorably realize a variety of circuits (such as a logic circuit or a driver circuit) which is required to operate at high speed.

A semiconductor device with a novel feature can be realized by including both the transistor including a material other than an oxide semiconductor and the transistor including an oxide semiconductor.

BRIEF DESCRIPTION OF DRAWINGS

In the accompanying drawings:
FIGS. 1A-1 and 1A-2 are a circuit diagram and a conceptual diagram of a semiconductor device;
FIG. 2 is a circuit diagram of a semiconductor device;
FIG. 3 is a timing chart;
FIG. 4 is a circuit diagram of a semiconductor device;
FIG. 5 is a circuit diagram of a semiconductor device;
FIG. 6 is a circuit diagram of a semiconductor device;
FIG. 7 is a circuit diagram of a semiconductor device;
FIGS. 8A and 8B are a cross-sectional view and a plan view, respectively, of a semiconductor device;
FIGS. 9A to 9H are cross-sectional views of a manufacturing process of a semiconductor device;
FIGS. 10A to 10E are cross-sectional views of a manufacturing process of a semiconductor device;
FIGS. 11A and 11B are a cross-sectional view and a plan view, respectively, of a semiconductor device;
FIGS. 12A to 12D are cross-sectional views of a manufacturing process of a semiconductor device;
FIGS. 13A and 13B are a cross-sectional view and a plan view, respectively, of a semiconductor device;
FIGS. 14A to 14D are cross-sectional views of a manufacturing process of a semiconductor device;
FIGS. 15A to 15C are cross-sectional views of a manufacturing process of a semiconductor device;
FIGS. 16A to 16F are diagrams illustrating electronic devices each including a semiconductor device;
FIG. 17 is a graph showing examination results of a memory window width;
FIG. 18 is a graph showing characteristics of a transistor including an oxide semiconductor;
FIG. 19 is a diagram of a circuit for evaluating characteristics of a transistor including an oxide semiconductor;
FIG. 20 is a timing chart for evaluating characteristics of a transistor including an oxide semiconductor;
FIG. 21 is a graph showing characteristics of a transistor including an oxide semiconductor;
FIG. 22 is a graph showing characteristics of a transistor including an oxide semiconductor;
FIGS. 23A and 23B are a cross-sectional view and a plan view, respectively, of a semiconductor device; and

FIGS. **24**A to **24**D are cross-sectional views of a manufacturing process of a semiconductor device.

## BEST MODE FOR CARRYING OUT THE INVENTION

Hereinafter, examples of embodiments of the present invention will be described with reference to the drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be construed as being limited to the description in the following embodiments and examples.

Note that for the easy understanding, the position, size, range, and the like of each component illustrated in the drawings and the like are not actual ones in some cases. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like disclosed in the drawings and the like.

In this specification and the like, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components, and the terms do not limit the components numerically.

### Embodiment 1

In this embodiment, a circuit configuration and operation of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. **1**A-**1** and **1**A-**2**. Note that in circuit diagrams, "OS" may be written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

In the semiconductor device illustrated in FIG. **1**A-**1**, a first wiring (a 1st Line, also referred to as a source line) is electrically connected to a source electrode of a transistor **160**, and a second wiring (a 2nd Line, also referred to as a bit line) is electrically connected to a drain electrode of the transistor **160**. A third line (a 3rd Line, also referred to as a first signal line) and one of a source electrode and a drain electrode of a transistor **162** are electrically connected to each other, and a fourth line (a 4th Line, also referred to as a second signal line) and a gate electrode of the transistor **162** are electrically connected to each other. A gate electrode of the transistor **160** and the other of the source electrode and the drain electrode of the transistor **162** are electrically connected to one electrode of a capacitor **164**. A fifth line (a 5th Line, also referred to as a word line) and the other electrode of the capacitor **164** are electrically connected to each other.

Here, a transistor including an oxide semiconductor is used as the transistor **162**. A transistor including an oxide semiconductor has a characteristic of significantly small off-state current. Therefore, when the transistor **162** is turned off, a potential of the gate electrode of the transistor **160** can be held for an extremely long time. Provision of the capacitor **164** facilitates holding of electric charge given to the gate electrode of the transistor **160** and reading of stored data.

The semiconductor device illustrated in FIG. **1**A-**1** utilizes a characteristic in which the potential of the gate electrode of the transistor **160** can be held, thereby writing, storing, and reading data as follows.

First, writing and storing of data will be described. A potential of the fourth wiring is set to a potential at which the transistor **162** is turned on, so that the transistor **162** is turned on. Accordingly, a potential of the third wiring is supplied to the gate electrode of the transistor **160** and one electrode of

the capacitor **164**. That is, predetermined electric charge is given to the gate electrode of the transistor **160** (writing). Here, one of electric charges for supply of two different potentials (hereinafter referred to as a Low-level electric charge and a High-level electric charge) is given to the gate electrode of the transistor **160**. After that, the potential of the fourth wiring is set to a potential at which the transistor **162** is turned off, so that the transistor **162** is turned off. Thus, the electric charge given to the gate electrode of the transistor **160** is held (holding).

Since the off-state current of the transistor **162** is significantly small, the electric charge of the gate electrode of the transistor **160** is held for a long time.

Next, reading of data will be described. By supplying an appropriate potential (reading potential) to the fifth wiring while a predetermined potential (constant potential) is supplied to the first wiring, the potential of the second wiring varies depending on the amount of electric charge held in the gate electrode of the transistor **160**. This is because in general, when the transistor **160** is an n-channel transistor, apparent threshold voltage $V_{th\_H}$ in the case where the High-level electric charge is given to the gate electrode of the transistor **160** is lower than apparent threshold voltage $V_{th\_L}$ in the case where the Low-level electric charge is given to the gate electrode of the transistor **160**. Here, apparent threshold voltage refers to the potential of the fifth wiring, which is needed to turn on the transistor **160**. Thus, the potential of the fifth wiring is set to a potential $V_0$ intermediate between $V_{th\_H}$ and $V_{th\_L}$, whereby electric charge given to the gate electrode of the transistor **160** can be determined. For example, in the case where the High-level electric charge is given in writing, when the potential of the fifth wiring is set to $V_0$ ($>V_{th\_H}$), the transistor **160** is turned on. In the case where the Low-level electric charge is given in writing, even when the potential of the fifth wiring is set to $V_0$ ($<V_{th\_L}$), the transistor **160** remains in an off state. Therefore, the stored data can be read by the potential of the second wiring.

Note that in the case where memory cells are arrayed to be used, only data of desired memory cells needs to be read. In the memory cells where data are not read, a potential at which the transistor **160** is turned off regardless of a state of the gate electrode of the transistor **160**, that is, a potential lower than $V_{th\_H}$ may be supplied to the fifth wiring.

Next, rewriting of data will be described. Rewriting of data is performed in a manner similar to that of the writing and holding of data. That is, the potential of the fourth wiring is set to a potential at which the transistor **162** is turned on, so that the transistor **162** is turned on. Accordingly, the potential of the third wiring (potential related to new data) is supplied to the gate electrode of the transistor **160** and one electrode of the capacitor **164**. After that, the potential of the fourth wiring is set to a potential at which the transistor **162** is turned off, so that the transistor **162** is turned off. Accordingly, electric charge related to the new data is given to the gate electrode of the transistor **160**.

In the semiconductor device according to the disclosed invention, data can be directly rewritten by another writing of data in the above-described manner. Therefore, extracting of electric charge from a floating gate with the use of high voltage, which is needed in a flash memory or the like, is not necessary and thus reduction in operation speed, which is attributed to erasing operation, can be suppressed. In other words, high-speed operation of the semiconductor device can be realized.

Note that the source electrode or the drain electrode of the transistor **162** is electrically connected to the gate electrode of the transistor **160**, thereby having an effect similar to that of a

floating gate of a floating gate transistor used for a nonvolatile memory element. Therefore, a portion in the drawing where the source electrode or the drain electrode of the transistor **162** is electrically connected to the gate electrode of the transistor **160** is called a floating gate portion FG (or a node FG) in some cases. When the transistor **162** is off, the floating gate portion FG can be regarded as being embedded in an insulator and thus electric charge is held in the floating gate portion FG. The amount of off-state current of the transistor **162** including an oxide semiconductor is less than or equal to one hundred thousandth of the amount of off-state current of a transistor including silicon or the like; thus, loss of the electric charge accumulated in the floating gate portion FG due to leakage current in the transistor **162** is negligible. That is, with the transistor **162** including an oxide semiconductor, a nonvolatile storage device which can store data even when power is not supplied can be realized.

For example, when the off-state current of the transistor **162** is 10 zA/μm (1 zA (zeptoampere) is $1 \times 10^{-21}$ A) or less at room temperature and the capacitance value of the capacitor **164** is approximately 10 fF, data can be stored for $10^4$ seconds or longer. Needless to say, the holding time depends on transistor characteristics and the capacitance value.

Further, in that case, the problem of deterioration of a gate insulating film (tunnel insulating film), which is pointed out in a conventional floating gate transistor, does not exist. That is, the deterioration of a gate insulating film due to injection of an electron into a floating gate, which has been traditionally regarded as a problem, can be solved. This means that there is no limitation on the number of times of writing in principle. Furthermore, high voltage needed for writing or erasing in a conventional floating gate transistor is not necessary.

The components such as transistors in the semiconductor device in FIG. **1A-1** can be regarded as including a resistor and a capacitor as shown in FIG. **1A-2**. That is, in FIG. **1A-2**, the transistor **160** and the capacitor **164** are each regarded as including a resistor and a capacitor. R1 and C1 denote the resistance value and the capacitance value of the capacitor **164**, respectively. The resistance value R1 corresponds to the resistance value which depends on an insulating layer included in the capacitor **164**. R2 and C2 denote the resistance value and the capacitance value of the transistor **160**, respectively. The resistance value R2 corresponds to the resistance value which depends on a gate insulating layer at the time when the transistor **160** is on. The capacitance value C2 corresponds to the value of so-called gate capacitance (capacitance formed between the gate electrode and the source electrode or the drain electrode and capacitance formed between the gate electrode and the channel formation region).

An electron holding period (also referred to as a data holding period) is determined mainly by off-state current of the transistor **162** under the conditions that gate leakage of the transistor **162** is sufficiently small and that R1≧ROS and R2≧ROS are satisfied, where the resistance value (also referred to as effective resistance) between the source electrode and the drain electrode in the case where the transistor **162** is off is ROS.

On the other hand, when the conditions are not satisfied, it is difficult to secure sufficient holding period even if the off-state current of the transistor **162** is small enough. This is because leakage current other than the off-state current of the transistor **162** (e.g., leakage current generated between the source electrode and the gate electrode) is large. Thus, it can be said that the semiconductor device disclosed in this embodiment preferably satisfies the above relation.

It is preferable that C1≧C2 be satisfied. When C1 is larger, variation in the potential of the fifth wiring can be suppressed

when the potential of the floating gate portion FG is controlled by the fifth wiring (e.g., at the time of reading).

When the above relation is satisfied, a more favorable semiconductor device can be realized. Note that R1 and R2 are controlled by gate insulating layers of the transistor **160** and the transistor **162**. This is also applied to C1 and C2. Therefore, the material, the thickness, and the like of the gate insulating layers are preferably set as appropriate so that the above relation is satisfied.

In the semiconductor device described in this embodiment, the node FG has an effect similar to that of a floating gate of a floating gate transistor of a flash memory or the like, but the node FG of this embodiment has a feature which is essentially different from that of the floating gate of the flash memory or the like. In the case of a flash memory, since voltage applied to a control gate is high, it is necessary to keep a proper distance between cells in order to prevent the potential from affecting a floating gate of the adjacent cell. This is one of factors inhibiting high integration of the semiconductor device. The factor is attributed to a basic principle of a flash memory, in which tunneling current flows in applying a high electrical field.

Further, because of the above principle of a flash memory, deterioration of an insulating film proceeds and thus another problem of the limit on the number of times of rewriting (approximately $10^4$ to $10^5$ times) occurs.

The semiconductor device according to the disclosed invention is operated by switching of a transistor including an oxide semiconductor and does not use the above-described principle of electric charge injection by tunneling current. That is, a high electrical field for electric charge injection is not necessary unlike a flash memory. Accordingly, it is not necessary to consider an influence of a high electrical field from a control gate on an adjacent cell, which facilitates high integration.

Further, electric charge injection by tunneling current is not utilized, which means that there is no cause for deterioration of a memory cell. In other words, the semiconductor device according to the disclosed invention has higher durability and reliability than a flash memory.

In addition, it is also advantageous that a high electrical field is unnecessary and a large peripheral circuit (such as a booster circuit) is unnecessary, as compared to a flash memory.

In the case where the dielectric constant ∈r1 of the insulating layer included in the capacitor element **164** is different from the dielectric constant ∈r2 of the insulating layer forming a gate capacitor of the transistor **160**, it is easy to satisfy C1≧C2 while 2·S2≧S1 (preferably S2≧S1) is satisfied where S1 is the area of the insulating layer included in the capacitor element **164** and S2 is the area of the insulating layer forming the gate capacitor of the transistor **160**. That is, it is easy to satisfy C1≧C2 while it is satisfied that the area of the insulating layer included in the capacitor element **164** is small. Specifically, for example, a film formed of a high-k material such as hafnium oxide or a stack of a film formed of a high-k material such as hafnium oxide and a film formed of an oxide semiconductor is used for the insulating layer including in the capacitor element **164** so that ∈r1 can be set to 10 or more, preferably 15 or more, and silicon oxide is used for the insulating layer forming the gate capacitor of the transistor **160** so that ∈r2 can be set to 3 to 4.

Combination of such structures enables higher integration of the semiconductor device according to the disclosed invention.

Note that an n-channel transistor in which electrons are majority carriers is used in the above description; needless to

say, a p-channel transistor in which holes are majority carriers can be used instead of the n-channel transistor.

As described above, a semiconductor device according to an embodiment of the disclosed invention has a nonvolatile memory cell including a writing transistor where leakage current (off-state current) between a source and a drain is small in an off state, a reading transistor formed using a semiconductor material different from that of the writing transistor, and a capacitor.

The off-state current of the writing transistor is preferably less than or equal to 100 zA ($1\times10^{-19}$ A), more preferably less than or equal to 10 zA ($1\times10^{-20}$ A), still more preferably less than or equal to 1 zA ($1\times10^{-21}$ A) at ambient temperature (e.g., 25° C.). In the case of a transistor including silicon, it is difficult to achieve such small off-state current. However, in a transistor obtained by processing an oxide semiconductor under an appropriate condition, small off-state current can be achieved. Therefore, a transistor including an oxide semiconductor is preferably used as the writing transistor.

In addition, a transistor including an oxide semiconductor has a small subthreshold swing value (S value), so that the switching rate can be sufficiently high even if mobility is relatively low. Therefore, by using the transistor as the writing transistor, rising of a writing pulse given to the node FG can be very sharp. Further, off-state current is small and thus the amount of electric charge held in the node FG can be reduced. That is, by using a transistor including an oxide semiconductor as a writing transistor, rewriting of data can be performed at high speed.

As for the reading transistor, although there is no limitation on off-state current, it is preferable to use a transistor which operates at high speed in order to increase the reading rate. For example, a transistor with a switching rate of one nanosecond or faster is preferably used as the reading transistor.

Data is written to the memory cell by turning on the writing transistor so that a potential is supplied to a node where one of a source electrode and a drain electrode of the writing transistor, one electrode of the capacitor, and a gate electrode of the reading transistor are electrically connected to one another, and then turning off the writing transistor so that the predetermined amount of electric charge is held in the node. Here, the off-state current of the writing transistor is extremely small; thus, the electric charge supplied to the node is held for a long time. When off-state current is, for example, substantially 0, refresh operation needed for a conventional DRAM can be unnecessary or the frequency of refresh operation can be significantly low (e.g., about once a month or a year). Accordingly, power consumption of a semiconductor device can be reduced sufficiently.

Further, data can be rewritten directly by overwriting of new data to the memory cell. For that reason, erasing operation which is necessary for a flash memory or the like is not needed, so that reduction in operation speed due to erasing operation can be prevented. In other words, high-speed operation of the semiconductor device can be realized. Moreover, high voltage necessary for a conventional floating gate transistor to write and erase data is unnecessary; thus, power consumption of the semiconductor device can be further reduced. The highest voltage applied to the memory cell according to this embodiment (the difference between the highest potential and the lowest potential applied to respective terminals of the memory cell at the same time) can be 5 V or lower, preferably 3 V or lower, in each memory cell in the case where data of two stages (one bit) is written.

The memory cell provided in the semiconductor device according to the disclosed invention may include at least the writing transistor, the reading transistor, and the capacitor.

Further, the memory cell can operate even when the area of the capacitor is small. Accordingly, the area of each memory cell can be sufficiently small as compared to an SRAM which requires six transistors in each memory cell, for example; thus, the memory cells can be arranged in a semiconductor device at high density.

In a conventional floating gate transistor, electric charge travels in a gate insulating film (tunnel insulating film) during writing operation, so that deterioration of the gate insulating film (tunnel insulating film) cannot be avoided. In contrast, in the memory cell according to an embodiment of the present invention, data is written by switching operation of a writing transistor; therefore, the deterioration of a gate insulating film, which has been traditionally recognized as a problem, can be solved. This means that there is no limitation on the number of times of writing in principle and writing durability is very high. For example, in the memory cell according to an embodiment of the present invention, the current-voltage characteristic is not degraded even after data is written $1\times10^{9}$ or more times (one billion or more times).

Further, in the case of using a transistor including an oxide semiconductor as the writing transistor of the memory cell, the current-voltage characteristic of the memory cell is not degraded even at, for example, a high temperature of 150° C. because an oxide semiconductor generally has a wide energy gap of 3.0 eV to 3.5 eV and includes extremely few thermally excited carriers.

As a result of intensive research, the present inventors have succeeded in finding for the first time that a transistor including an oxide semiconductor has excellent characteristics in that the characteristics do not deteriorate even at a high temperature of 150° C. and off-state current is less than or equal to 100 zA, which is extremely small. According to an embodiment of the disclosed invention, a semiconductor device having a novel feature by using a transistor having such excellent characteristics as the writing transistor of the memory cell is provided.

Note that the structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

Embodiment 2

In this embodiment, an application example of the semiconductor device described in the above embodiment will be described. Specifically, an example of a semiconductor device in which the semiconductor devices described in the above embodiment are arranged in matrix will be described.

FIG. 2 is an example of a circuit diagram of a semiconductor device which has memory capacity of m×n bits.

The semiconductor device according to an embodiment of the present invention includes a memory cell array where m word lines WL, m second signal lines S2, n bit lines BL, n source lines SL, n first signal lines S1, and a plurality of memory cells 1100 are arranged in matrix of m (rows) (in a vertical direction)×n (columns) (in a horizontal direction) (m and n are natural numbers) and peripheral circuits such as a first driver circuit 1111, a second driver circuit 1112, a third driver circuit 1113, and a fourth driver circuit 1114. Here, the configuration described in the above embodiment (the configuration in FIG. 1A-1) is applied to the memory cell 1100.

That is, each of the memory cells 1100 includes a first transistor, a second transistor, and a capacitor. A gate electrode of the first transistor, one of a source electrode and a drain electrode of the second transistor, and one electrode of the capacitor are electrically connected to one another. The

source line SL and a source electrode of the first transistor are electrically connected to each other. The bit line BL and a drain electrode of the first transistor are electrically connected to each other. The first signal line S1 and the other of the source electrode and the drain electrode of the second transistor are electrically connected to each other. The second signal line S2 and a gate electrode of the second transistor are electrically connected to each other. The word line WL and the other electrode of the capacitor are electrically connected to each other.

Further, the memory cells 1100 are electrically connected in parallel between the source line SL and the bit line BL. For example, the memory cell 1100 of an i-th row and a j-th column (i,j) (i is an integer which is greater than or equal to 1 and less than or equal to m, and j is an integer which is greater than or equal to 1 and less than or equal to n) is electrically connected to the source line SL(j), the bit line BL(j), the first signal line S1(j), the word line WL(i), and the second signal line S2(i).

The source lines SL and the bit lines BL are electrically connected to the first driver circuit 1111. The first signal lines S1 are electrically connected to the second driver circuit 1112. The second signal lines S2 are electrically connected to the third driver circuit 1113. The word lines WL are electrically connected to the fourth driver circuit 1114. Note that here, the first driver circuit 1111, the second driver circuit 1112, the third driver circuit 1113, and the fourth driver circuit 1114 are separately provided; however, the disclosed invention is not limited to this. A decoder having any one or some of the functions may be used.

Next, writing operation and reading operation of the semiconductor device in FIG. 2 will be described with reference to a timing chart in FIG. 3.

Although operation of semiconductor devices of two rows and two columns will be described for simplification, the disclosed invention is not limited to this.

FIG. 3 is a chart illustrating operation of the semiconductor device in FIG. 2. In FIG. 3, S1(1) and S1(2) are potentials of the first signal lines S1; S2(1) and S2(2) are potentials of the second signal lines S2; BL(1) and BL(2) are potentials of the bit lines BL; WL(1) and WL(2) are potentials of the word lines WL; and SL(1) and SL(2) are potentials of the source lines SL.

First, writing data to the memory cell 1100 (1,1) and the memory cell 1100 (1,2) which are in the first row and reading data from the memory cell 1100 (1,1) and the memory cell 1100 (1,2) which are in the first row will be described. Note that in the following description, it is assumed that data to be written to the memory cell 1100 (1,1) is "1" and data to be written to the memory cell 1100 (1,2) is "0".

First, the writing will be described. In a writing period of the first row, a potential $V_H$ is supplied to the second signal line S2(1) of the first row so that the second transistors of the first row are turned on. Further, a potential 0 V is supplied to the second signal line S2(2) of the second row so that the second transistors of the second row are turned off.

Next, a potential $V_2$ and a potential 0 V are supplied to the first signal line S1(1) of the first column and the first signal line S1(2) of the second column, respectively.

As a result, the potential $V_2$ and the potential 0 V are applied to a floating gate portion FG of the memory cell 1100 (1,1) and a floating gate portion FG of the memory cell 1100 (1,2), respectively. Here, the potential $V_2$ is higher than the threshold voltage of the first transistors. Then, the potential of the second signal line S2(1) of the first row is set to 0 V so that the second transistors of the first row are turned off. Thus, writing is completed.

Note that the word lines WL(1) and WL(2) are set at 0 V. Further, before the potential of the first signal line S1(1) of the first column is changed to 0 V, the potential of the second signal line S2(1) of the first row is set to 0 V. The threshold voltage of a memory element to which data has been written is $V_{w0}$ in the case of data "0" and $V_{w1}$ in the case of data "1", assuming that a terminal electrically connected to the word line WL is a control gate electrode, the source electrode of the first transistor is a source electrode, and the drain electrode of the second transistor is a drain electrode, in the memory element. Here, the threshold voltage of the memory cell means voltage of the terminal connected to the word line WL, which changes resistance between the source electrode and the drain electrode of the first transistor. Note that $V_{w0} > 0 > V_{w1}$ is satisfied.

Then, the reading will be described. In a reading period of the first row, a potential 0 V and a potential $V_L$ are supplied to the word line WL(1) of the first row and the word line WL(2) of the second row, respectively. The potential $V_L$ is lower than the threshold voltage $V_1$. When WL(1) is at a potential of 0 V, in the first row, the first transistor of the memory cell in which data "0" is stored is off, and the first transistor of the memory cell in which data "1" is stored is on. When the word line WL(2) is at the potential $V_L$, in the second row, the second transistors of the memory cells in which either data "0" or data "1" is stored are off.

Next, a potential 0 V is supplied to the source line SL(1) of the first column and the source line SL(2) of the second column.

As a result, the transistor of the memory cell 1100 (1,1) between the bit line BL(1) and the source line SL(1) is turned on, thereby having low resistance, and the transistor of the memory cell between the bit line BL(2) and the source line SL(2) is turned off, thereby having high resistance. A reading circuit connected to the bit line BL(1) and the bit line BL(2) can read data on the basis of a difference in resistance between the bit lines BL.

Further, a potential 0 V and the potential $V_L$ are supplied to the second signal line S2(1) and the second signal line S2(2), respectively, so that all the second transistors are turned off. The potential of the floating gate portion FG of the first row is 0 V or $V_2$; thus, the potential of the second signal line S2(1) is set to 0 V, whereby both of the second transistors of the first row can be turned off. On the other hand, the potential of the floating gate portion FG of the second row is lower than the potential at the time directly after data writing if the potential $V_L$ is supplied to the word line WL(2). Therefore, in order to prevent the second transistor from being turned on, the potential of the second signal line S2(2) is set to low similarly to the potential of the word line WL(2). Thus, all the second transistors can be turned off.

Next, a reading circuit included in the first driver circuit 1111 is illustrated in FIG. 4. The reading circuit is connected to the memory cell through the bit line BL. In addition, the reading circuit includes a transistor whose gate electrode and source or drain electrode are connected to $V_{dd}$, and a clocked inverter. An output potential in the case where the circuit in FIG. 4 is used will be described. Here, the case where the reading circuit in FIG. 4 is connected to each of the bit lines BL(1) and BL(2) will be described. Since the resistance between the bit line BL(1) and the source line SL(1) is low, a low potential is supplied to the clocked inverter and an output D(1) is a signal High. Since the resistance between the bit line BL(2) and the source line SL(2) is high, a high potential is supplied to the clocked inverter and an output D(2) is a signal Low.

As for the operating voltage, it can be assumed that, for example, $V_{dd}=2$ V, $V_2=1.5$ V, $V_H=2$ V, and $V_L=-2$ V are satisfied.

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

## Embodiment 3

In this embodiment, another example of a semiconductor device in which the semiconductor devices described in the above embodiment are arranged in matrix will be described.

FIG. 5 illustrates an example of a circuit of a semiconductor device which has memory capacity of m×n bits.

The semiconductor device in FIG. 5 includes a memory cell array where m word lines WL, m first signal lines S1, n bit lines BL, n source lines SL, n second signal lines S2, and the plurality of memory cells 1100 are arranged in matrix of m (rows) (in a vertical direction)×n (columns) (in a horizontal direction) (m and n are natural numbers) and peripheral circuits such as the first driver circuit 1111, the second driver circuit 1112, the third driver circuit 1113, and the fourth driver circuit 1114. Here, the configuration described in the above embodiment (the configuration in FIG. 1A-1) is applied to the memory cell 1100.

Further, each of the memory cells 1100 includes a first transistor, a second transistor, and a capacitor. A gate electrode of the first transistor, one of a source electrode and a drain electrode of the second transistor, and one electrode of the capacitor are electrically connected to one another. The source line SL and a source electrode of the first transistor are electrically connected to each other. The bit line BL and a drain electrode of the first transistor are electrically connected to each other. The first signal line S1 and the other of the source electrode and the drain electrode of the second transistor are electrically connected to each other. The second signal line S2 and a gate electrode of the second transistor are electrically connected to each other. The word line WL and the other electrode of the capacitor are electrically connected to each other.

In FIG. 5, the memory cell 1100 of an i-th row and a j-th column (i,j) (i is an integer which is greater than or equal to 1 and less than or equal to m, and j is an integer which is greater than or equal to 1 and less than or equal to n) is electrically connected to the source line SL(j), the bit line BL(j), the word line WL(i), the first signal line S1($i$), and the second signal line S2($j$).

In FIG. 5, the bit lines BL and the source lines SL are electrically connected to the first driver circuit 1111. The second signal lines S2 are electrically connected to the second driver circuit 1112. The first signal lines S1 are electrically connected to the third driver circuit 1113. The word lines WL are electrically connected to the fourth driver circuit 1114.

FIG. 6 is an example of a circuit diagram of a semiconductor device having memory capacity of m×n bits, which is partly different from that of FIG. 5.

The semiconductor device in FIG. 6 includes a memory cell array where m bit lines BL, m source lines SL, m second signal lines S2, n word lines WL, n first signal lines S1, and the plurality of memory cells 1100 are arranged in matrix of m (rows) (in a vertical direction)×n (columns) (in a horizontal direction) (m and n are natural numbers) and peripheral circuits such as the first driver circuit 1111, the second driver circuit 1112, the third driver circuit 1113, and the fourth driver circuit 1114. Here, the configuration described in the

above embodiment (the configuration in FIG. 1A-1) is applied to the memory cell 1100.

In FIG. 6, the memory cell 1100 of an i-th row and a j-th column (i,j) (i is an integer which is greater than or equal to 1 and less than or equal to m, and j is an integer which is greater than or equal to 1 and less than or equal to n) is electrically connected to the bit line BL(i), the source line SL(i), the second signal line S2($i$), the word line WL(j), and the first signal line S1($j$).

In FIG. 6, the word lines WL are electrically connected to the first driver circuit 1111. The first signal lines S1 are electrically connected to the second driver circuit 1112. The second signal lines S2 are electrically connected to the third driver circuit 1113. The bit lines BL and the source lines SL are electrically connected to the fourth driver circuit 1114.

A semiconductor device in FIG. 7 includes a memory cell array where m bit lines BL, m source lines SL, m first signal lines S1, n word lines WL, n second signal lines S2, and the plurality of memory cells 1100 are arranged in matrix of m (rows) (in a vertical direction)×n (columns) (in a horizontal direction) (m and n are natural numbers) and peripheral circuits such as the first driver circuit 1111, the second driver circuit 1112, the third driver circuit 1113, and the fourth driver circuit 1114. Here, the configuration described in the above embodiment (the configuration in FIG. 1A-1) is applied to the memory cell 1100.

In FIG. 7, the memory cell 1100 of an i-th row and a j-th column (i,j) (i is an integer which is greater than or equal to 1 and less than or equal to m, and j is an integer which is greater than or equal to 1 and less than or equal to n) is electrically connected to the source line SL(i), the bit line BL(i), the word line WL (j), the first signal line S1($i$), and the second signal line S2($j$).

In FIG. 7, the word lines WL are electrically connected to the first driver circuit 1111. The second signal lines S2 are electrically connected to the second driver circuit 1112. The first signal lines S1 are electrically connected to the third driver circuit 1113. The bit lines BL and the source lines SL are electrically connected to the fourth driver circuit 1114.

Note that the operation of the circuits of the semiconductor devices in FIG. 5, FIG. 6, and FIG. 7 is similar to the operation of the circuit of the semiconductor device in FIG. 2; therefore, the detailed description is omitted. The timing chart of FIG. 3 may be referred to for the operation of the circuits of the semiconductor devices in FIG. 5, FIG. 6, and FIG. 7. In addition, FIG. 4 can be referred to for reading circuits used in the semiconductor devices in FIG. 5, FIG. 6, and FIG. 7.

By using an oxide semiconductor whose off-state current is extremely small for the semiconductor devices in FIG. 5, FIG. 6, and FIG. 7, stored data can be retained for an extremely long time. In other words, power consumption can be sufficiently reduced because refresh operation is unnecessary or the frequency of refresh operation can be extremely low. Moreover, stored data can be retained for a long time even when power is not supplied.

Further, in the semiconductor devices in FIG. 5, FIG. 6, and FIG. 7, high voltage is not needed to write data, and deterioration of the element does not become a problem. Therefore, each of the semiconductor devices in FIG. 5, FIG. 6, and FIG. 7 has no limitation on the number of times of rewriting which is a problem of a conventional nonvolatile memory, and reliability thereof is drastically improved. Further, writing of data is performed depending on an on state and an off state of the transistor, so that high-speed operation can be easily realized. Additionally, there is an advantage that operation for erasing data is not needed.

Further, since a transistor including a material other than an oxide semiconductor can operate at sufficiently high speed, combination of this transistor with a transistor including an oxide semiconductor enables high speed of operation (e.g., reading operation of data) of a semiconductor device to be sufficiently secured. Furthermore, with the transistor including a material other than an oxide semiconductor, a variety of circuits (such as a logic circuit and a driver circuit) which need to operate at high speed can be favorably realized.

Thus, a semiconductor device with a novel feature can be realized by including both the transistor including a material other than an oxide semiconductor and the transistor including an oxide semiconductor.

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

Embodiment 4

In this embodiment, a structure and a manufacturing method of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 8A and 8B, FIGS. 9A to 9H, and FIGS. 10A to 10E.
<Cross-Sectional Structure and Planar Structure of Semiconductor Device>

FIGS. 8A and 8B illustrate an example of a structure of a semiconductor device. FIG. 8A illustrates a cross section of the semiconductor device, and FIG. 8B illustrates a plan view of the semiconductor device. Here, FIG. 8A corresponds to a cross section along line A1-A2 and line B1-B2 in FIG. 8B. The semiconductor device illustrated in FIGS. 8A and 8B includes the transistor 160 including a material other than an oxide semiconductor in a lower portion, and the transistor 162 including an oxide semiconductor in an upper portion. A transistor including a material other than an oxide semiconductor can operate at high speed easily. On the other hand, a transistor including an oxide semiconductor can hold electric charge for a long time owing to its characteristics.

Although both of the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. Since the technical nature of the disclosed invention is to use an oxide semiconductor in the transistor 162 so that data can be stored, it is not necessary to limit a specific structure of a semiconductor device to the structure described here.

The transistor 160 in FIGS. 8A and 8B includes a channel formation region 116 provided in a substrate 100 including a semiconductor material (e.g., silicon), impurity regions 114 and high-concentration impurity regions 120 (these regions are also collectively referred to simply as impurity regions) provided so that the channel formation region 116 is sandwiched therebetween, a gate insulating layer 108 provided over the channel formation region 116, a gate electrode 110 provided over the gate insulating layer 108, and a source or drain electrode 130a and a source or drain electrode 130b electrically connected to the impurity regions 114.

A sidewall insulating layer 118 is provided on a side surface of the gate electrode 110. The high-concentration impurity region 120 is positioned in a region of the substrate 100, which does not overlap with the sidewall insulating layer 118 when seen from a direction perpendicular to the surface of the substrate 100. A metal compound region 124 is positioned in contact with the high-concentration impurity region 120. An element isolation insulating layer 106 is provided over the substrate 100 so as to surround the transistor 160. An inter-

layer insulating layer 126 and an interlayer insulating layer 128 are provided so as to cover the transistor 160. Each of the source or drain electrode 130a and the source or drain electrode 130b is electrically connected to the metal compound region 124 through an opening formed in the interlayer insulating layer 126 and the interlayer insulating layer 128. That is, each of the source or drain electrode 130a and the source or drain electrode 130b is electrically connected to the high-concentration impurity region 120 and the impurity region 114 through the metal compound region 124. Further, an electrode 130c is electrically connected to the gate electrode 110 through an opening formed in the interlayer insulating layer 126 and the interlayer insulating layer 128. Note that the sidewall insulating layer 118 is not formed in some cases for integration of the transistor 160 or the like.

The transistor 162 in FIGS. 8A and 8B includes a source or drain electrode 142a and a source or drain electrode 142b which are provided over the interlayer insulating layer 128; an oxide semiconductor layer 144 which is electrically connected to the source or drain electrode 142a and the source or drain electrode 142b; a gate insulating layer 146 which covers the source or drain electrode 142a, the source or drain electrode 142b, and the oxide semiconductor layer 144; and a gate electrode 148a which is provided over the gate insulating layer 146 so as to overlap with the oxide semiconductor layer 144. Here, the gate electrode 110 of the transistor 160 is electrically connected to the source or drain electrode 142a of the transistor 162 through the electrode 130c.

Here, it is preferable that the oxide semiconductor layer 144 be purified by sufficient removal of impurities such as hydrogen or sufficient supply of oxygen. Specifically, the concentration of hydrogen in the oxide semiconductor layer 144 is lower than or equal to $5 \times 10^{19}$ atoms/cm$^3$, preferably lower than or equal to $5 \times 10^{18}$ atoms/cm$^3$, more preferably lower than or equal to $5 \times 10^{17}$ atoms/cm$^3$, for example. Note that the concentration of hydrogen in the oxide semiconductor layer 144 is measured by secondary ion mass spectrometry (SIMS). Thus, in the oxide semiconductor layer 144 in which the hydrogen concentration is sufficiently reduced so that the oxide semiconductor layer is purified and defect levels in the energy gap due to oxygen deficiency are reduced by sufficient supply of oxygen, the carrier density is lower than $1 \times 10^{12}$/cm$^3$, preferably lower than $1 \times 10^{11}$/cm$^3$, more preferably lower than $1.45 \times 10^{10}$/cm$^3$. For example, the off-state current (here, current per micrometer of channel width) at room temperature is less than or equal to 100 zA/μm (1 zA (zeptoampere) is $1 \times 10^{-21}$ A), preferably less than or equal to 10 zA/μm. With the use of such an i-type (intrinsic) or substantially i-type oxide semiconductor, the transistor 162 which has extremely excellent off-current characteristics can be obtained.

Note that in the transistor 162 in FIGS. 8A and 8B, the oxide semiconductor layer 144 is not processed into an island shape; therefore, contamination of the oxide semiconductor layer 144 due to etching in the processing can be prevented.

The capacitor 164 includes the source or drain electrode 142a, the oxide semiconductor layer 144, the gate insulating layer 146, and an electrode 148b. That is, the source or drain electrode 142a functions as one electrode of the capacitor 164, and the electrode 148b functions as the other electrode of the capacitor 164.

Note that in the capacitor 164 in FIGS. 8A and 8B, the oxide semiconductor layer 144 and the gate insulating layer 146 are stacked, whereby insulation between the source or drain electrode 142a and the electrode 148b can be sufficiently secured.

Note that in the transistor 162 and the capacitor 164, end portions of the source or drain electrode 142a and the source or drain electrode 142b are preferably tapered. Here, the taper angle is greater than or equal to 30° and less than or equal to 60°, for example. Note that the taper angle is a tilt angle formed by a side surface and a bottom surface of a layer having a tapered shape (e.g., the source or drain electrode 142a) in the case where the layer is observed from a direction perpendicular to a cross section (a plane perpendicular to the surface of a substrate). The end portions of the source or drain electrode 142a and the source or drain electrode 142b are tapered, whereby coverage with the oxide semiconductor layer 144 can be improved and disconnection can be prevented.

Further, an interlayer insulating layer 150 is provided over the transistor 162 and the capacitor 164, and an interlayer insulating layer 152 is provided over the interlayer insulating layer 150.

<Method for Manufacturing Semiconductor Device>

Next, an example of a method for manufacturing the semiconductor device will be described. First, a method for manufacturing the transistor 160 in the lower portion will be described below with reference to FIGS. 9A to 9H, and then a method for manufacturing the transistor 162 in the upper portion will be described with reference to FIGS. 10A to 10E.

<Method for Manufacturing Transistor in Lower Portion>

First, the substrate 100 including a semiconductor material is prepared (see FIG. 9A). As the substrate 100 including a semiconductor material, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like; a compound semiconductor substrate made of silicon germanium or the like; an SOI substrate; or the like can be used. Here, an example of using a single crystal silicon substrate as the substrate 100 including a semiconductor material is described. Note that in general, the term "SOI substrate" means a substrate where a silicon layer is provided on an insulating surface. In this specification and the like, the term "SOI substrate" also means a substrate where a semiconductor layer including a material other than silicon is provided on an insulating surface. That is, a semiconductor layer included in the "SOI substrate" is not limited to a silicon layer. Moreover, the SOI substrate can be a substrate having a structure in which a semiconductor layer is provided over an insulating substrate such as a glass substrate with an insulating layer positioned therebetween.

A protective layer 102 serving as a mask for forming an element isolation insulating layer is formed over the substrate 100 (see FIG. 9A). As the protective layer 102, an insulating layer formed using a material such as silicon oxide, silicon nitride, or silicon oxynitride can be used, for example. Note that before or after this step, an impurity element imparting n-type conductivity or an impurity element imparting p-type conductivity may be added to the substrate 100 in order to control the threshold voltage of the transistor. When the semiconductor material included in the substrate 100 is silicon, phosphorus, arsenic, or the like can be used as the impurity imparting n-type conductivity. Boron, aluminum, gallium, or the like can be used as the impurity imparting p-type conductivity.

Next, part of the substrate 100 in a region that is not covered with the protective layer 102 (in an exposed region) is removed by etching with the use of the protective layer 102 as a mask. Thus, a semiconductor region 104 isolated from the other semiconductor regions is formed (see FIG. 9B). As the etching, dry etching is preferably performed, but wet etching

may be performed. An etching gas and an etchant can be selected as appropriate in accordance with a material to be etched.

Then, an insulating layer is formed so as to cover the semiconductor region 104, and the insulating layer in a region overlapping with the semiconductor region 104 is selectively removed, so that the element isolation insulating layer 106 is formed (see FIG. 9B). The insulating layer is formed using silicon oxide, silicon nitride, silicon oxynitride, or the like. As a method for removing the insulating layer, there are etching treatment and polishing treatment such as CMP treatment, and any of them can be employed. Note that the protective layer 102 is removed after the formation of the semiconductor region 104 or after the formation of the element isolation insulating layer 106.

Next, an insulating layer is formed over the semiconductor region 104, and a layer including a conductive material is formed over the insulating layer.

The insulating layer serves as a gate insulating layer later, and the insulating layer preferably has a single-layer structure or a stacked structure using a film including any of silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x>0$, $y>0$)), hafnium silicate ($HfSi_xO_y$ ($x>0$, $y>0$)) to which nitrogen is added, hafnium aluminate ($HfAl_xO_y$ ($x>0$, $y>0$)) to which nitrogen is added, and the like formed by a CVD method, a sputtering method, or the like. Alternatively, the insulating layer may be formed in such a manner that a surface of the semiconductor region 104 is oxidized or nitrided by high-density plasma treatment or thermal oxidation treatment. The high-density plasma treatment can be performed using, for example, a mixed gas of a rare gas such as He, Ar, Kr, or Xe and a gas such as oxygen, nitrogen oxide, ammonia, nitrogen, or hydrogen. The insulating layer can have a thickness of, for example, greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

The layer including a conductive material can be formed using a metal material such as aluminum, copper, titanium, tantalum, or tungsten. The layer including a conductive material may be formed using a semiconductor material such as polycrystalline silicon. There is no particular limitation on the method for forming the layer including a conductive material, and a variety of film formation methods such as an evaporation method, a CVD method, a sputtering method, and a spin coating method can be employed. Note that in this embodiment, an example of the case where the layer including a conductive material is formed using a metal material is described.

After that, the insulating layer and the layer including a conductive material are selectively etched, so that the gate insulating layer 108 and the gate electrode 110 are formed (see FIG. 9C).

Next, an insulating layer 112 that covers the gate electrode 110 is formed (see FIG. 9C). Then, the impurity regions 114 with a shallow junction depth are formed by adding phosphorus (P), arsenic (As), or the like to the semiconductor region 104 (see FIG. 9C). Note that phosphorus or arsenic is added here in order to form an n-channel transistor; an impurity element such as boron (B) or aluminum (Al) may be added in the case of forming a p-channel transistor. With the formation of the impurity regions 114, the channel formation region 116 is formed in the semiconductor region 104 below the gate insulating layer 108 (see FIG. 9C). Here, the concentration of the impurity added can be set as appropriate; however, the concentration is preferably increased when the size of a semiconductor element is extremely reduced. The step in which

the impurity regions 114 are formed after the formation of the insulating layer 112 is employed here; alternatively, the insulating layer 112 may be formed after the formation of the impurity regions 114.

Next, the sidewall insulating layer 118 is formed (see FIG. 9D). An insulating layer is formed so as to cover the insulating layer 112 and then subjected to highly anisotropic etching treatment, whereby the sidewall insulating layer 118 can be formed in a self-aligned manner. At this time, it is preferable to etch the insulating layer 112 partly so that a top surface of the gate electrode 110 and top surfaces of the impurity regions 114 are exposed. Note that the sidewall insulating layer 118 is not formed in some cases for the purpose of high integration or the like.

Then, an insulating layer is formed so as to cover the gate electrode 110, the impurity regions 114, the sidewall insulating layer 118, and the like. Next, phosphorus (P), arsenic (As), or the like is added to regions where the insulating layer is in contact with the impurity regions 114, so that the high-concentration impurity regions 120 are formed (see FIG. 9E). After that, the insulating layer is removed, and a metal layer 122 is formed so as to cover the gate electrode 110, the sidewall insulating layer 118, the high-concentration impurity regions 120, and the like (see FIG. 9E). A variety of film formation methods such as a vacuum evaporation method, a sputtering method, and a spin coating method can be employed for forming the metal layer 122. The metal layer 122 is preferably formed using a metal material that reacts with a semiconductor material included in the semiconductor region 104 to be a low-resistance metal compound. Examples of such a metal material are titanium, tantalum, tungsten, nickel, cobalt, and platinum.

Next, heat treatment is performed so that the metal layer 122 reacts with the semiconductor material. Thus, the metal compound regions 124 that are in contact with the high-concentration impurity regions 120 are formed (see FIG. 9F). Note that when the gate electrode 110 is formed using polycrystalline silicon or the like, a metal compound region is also formed in a region of the gate electrode 110 in contact with the metal layer 122.

As the heat treatment, irradiation with a flash lamp can be employed, for example. Although it is needless to say that another heat treatment method may be used, a method by which heat treatment for an extremely short time can be achieved is preferably used in order to improve the controllability of chemical reaction in formation of the metal compound. Note that the metal compound regions are formed by reaction of the metal material and the semiconductor material and have sufficiently high conductivity. The formation of the metal compound regions can sufficiently reduce electric resistance and improve element characteristics. Note that the metal layer 122 is removed after the metal compound regions 124 are formed.

Then, the interlayer insulating layer 126 and the interlayer insulating layer 128 are formed so as to cover the components formed in the above steps (see FIG. 9G). The interlayer insulating layer 126 and the interlayer insulating layer 128 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, or tantalum oxide. Moreover, the interlayer insulating layer 126 and the interlayer insulating layer 128 can be formed using an organic insulating material such as polyimide or acrylic resin. Note that a stacked structure of the interlayer insulating layer 126 and the interlayer insulating layer 128 is employed here; however, an embodiment of the disclosed invention is not limited to this. A single-layer structure or a stacked structure

including three or more layers can also be employed. After the formation of the interlayer insulating layer 128, a surface thereof is preferably planarized by CMP treatment, etching treatment, or the like.

Then, openings that reach the metal compound regions 124 are formed in the interlayer insulating layers, and the source or drain electrode 130a and the source or drain electrode 130b are formed in the openings (see FIG. 9H). The source or drain electrode 130a and the source or drain electrode 130b can be formed in such a manner, for example, that a conductive layer is formed in a region including the openings by a PVD method, a CVD method, or the like and then part of the conductive layer is removed by etching treatment, CMP treatment, or the like.

Specifically, it is possible to employ a method, for example, in which a thin titanium film is formed in a region including the openings by a PVD method, a thin titanium nitride film is formed by a CVD method, and then a tungsten film is formed so as to be embedded in the openings. Here, the titanium film formed by a PVD method has a function of reducing an oxide film (such as a natural oxide film) formed on a surface over which the titanium film is formed, thereby lowering the contact resistance with the lower electrodes or the like (the metal compound regions 124, here). The titanium nitride film formed after the formation of the titanium film has a barrier function of preventing diffusion of the conductive material. A copper film may be formed by a plating method after the formation of the barrier film of titanium, titanium nitride, or the like.

Note that in the case where the source or drain electrode 130a and the source or drain electrode 130b are formed by removing part of the conductive layer, processing is preferably performed so that the surfaces are planarized. For example, when a thin titanium film or a thin titanium nitride film is formed in a region including the openings and then a tungsten film is formed so as to be embedded in the openings, excess tungsten, titanium, titanium nitride, or the like can be removed and the planarity of the surface can be improved by subsequent CMP treatment. The surface including the source or drain electrode 130a and the source or drain electrode 130b is planarized in such a manner, so that an electrode, a wiring, an insulating layer, a semiconductor layer, and the like can be favorably formed in later steps.

Note that only the source or drain electrode 130a and the source or drain electrode 130b in contact with the metal compound regions 124 are shown here; however, an electrode that is in contact with the gate electrode 110 and the like can also be formed in this step. There is no particular limitation on a material used for the source or drain electrode 130a and the source or drain electrode 130b, and a variety of conductive materials can be used. For example, a conductive material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium can be used. In consideration of heat treatment performed later, it is preferable that the source or drain electrode 130a and the source or drain electrode 130b be formed using a material with heat resistance enough to withstand the heat treatment.

Through the above steps, the transistor 160 using the substrate 100 including a semiconductor material is formed (see FIG. 9H). The transistor 160 including a material other than an oxide semiconductor can operate at high speed.

Note that an electrode, a wiring, an insulating layer, or the like may be further formed after the above step. When the wiring has a multi-layer structure including a stacked structure of an interlayer insulating layer and a conductive layer, a highly integrated semiconductor device can be provided.

<Method for Manufacturing Transistor in Upper Portion>

Next, steps of manufacturing the transistor **162** over the interlayer insulating layer **128** will be described with reference to FIGS. **10A** to **10E**. Note that FIGS. **10A** to **10E** illustrate steps of manufacturing electrodes, the transistor **162**, and the like over the interlayer insulating layer **128**; therefore, the transistor **160** and the like positioned below the transistor **162** are omitted.

First, a conductive layer is formed over the interlayer insulating layer **128** and etched selectively, so that the source or drain electrode **142***a* and the source or drain electrode **142***b* are formed (see FIG. **10A**).

The conductive layer can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. As a material for the conductive layer, an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; an alloy including any of these elements as a component; or the like can be used. Any of manganese, magnesium, zirconium, and beryllium, or a material including two or more of these in combination may be used. Aluminum combined with an element selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium, or a material including two or more of these in combination may be used.

The conductive layer may have a single-layer structure or a stacked structure including two or more layers. For example, a single-layer structure of a titanium film or a titanium nitride film, a single-layer structure of an aluminum film including silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a two-layer structure in which a titanium film is stacked over a titanium nitride film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order, and the like can be given. Note that in the case where the conductive layer has the single-layer structure of a titanium film or a titanium nitride film, there is an advantage that the source or drain electrode **142***a* and the source or drain electrode **142***b* can be easily processed to be tapered.

Alternatively, the conductive layer may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide ($In_2O_3$), tin oxide ($SnO_2$), zinc oxide (ZnO), an indium oxide-tin oxide alloy ($In_2O_3$—$SnO_2$, which is abbreviated to ITO in some cases), an indium oxide-zinc oxide alloy ($In_2O_3$—ZnO), or any of these metal oxide materials including silicon or silicon oxide can be used.

The conductive layer is preferably etched so that end portions of the source or drain electrode **142***a* and the source or drain electrode **142***b* are tapered. Here, the taper angle is preferably greater than or equal to 30° and less than or equal to 60°, for example. The etching is performed so that the end portions of the source or drain electrode **142***a* and the source or drain electrode **142***b* are tapered, whereby coverage with the gate insulating layer **146** formed later can be improved and disconnection can be prevented.

The channel length (L) of the transistor is determined by a distance between a lower edge portion of the source or drain electrode **142***a* and a lower edge portion of the source or drain electrode **142***b*. Note that for light exposure for forming a mask used in the case where a transistor with a channel length (L) of less than 25 nm is formed, it is preferable to use extreme ultraviolet rays whose wavelength is as short as several nanometers to several tens of nanometers. The resolution of light exposure with extreme ultraviolet rays is high and the depth of focus is large. For these reasons, the channel length (L) of the transistor formed later can be greater than or equal to 10 nm and less than or equal to 1000 nm (1 μm), and the

circuit can operate at higher speed. Moreover, power consumption of the semiconductor device can be reduced by miniaturization.

Note that an insulating layer functioning as a base may be provided over the interlayer insulating layer **128**. The insulating layer can be formed by a PVD method, a CVD method, or the like.

Further, an insulating layer may be formed over the source or drain electrode **142***a* and the source or drain electrode **142***b*. By providing the insulating layer, parasitic capacitance between a gate electrode formed later and the source and drain electrodes **142***a* and **142***b* can be reduced.

After that, the oxide semiconductor layer **144** is formed so as to cover the source or drain electrode **142***a* and the source or drain electrode **142***b* (see FIG. **10B**).

As the oxide semiconductor layer **144**, an oxide of four metal elements such as an In—Sn—Ga—Zn—O-based oxide semiconductor, an oxide of three metal elements such as an In—Ga—Zn—O-based oxide semiconductor, an In—Sn—Zn—O-based oxide semiconductor, an In—Al—Zn—O-based oxide semiconductor, a Sn—Ga—Zn—O-based oxide semiconductor, an Al—Ga—Zn—O-based oxide semiconductor, or a Sn—Al—Zn—O-based oxide semiconductor, an oxide of two metal elements such as an In—Zn—O-based oxide semiconductor, a Sn—Zn—O-based oxide semiconductor, an Al—Zn—O-based oxide semiconductor, a Zn—Mg—O-based oxide semiconductor, a Sn—Mg—O-based oxide semiconductor, or an In—Mg—O-based oxide semiconductor, an In—O-based oxide semiconductor, a Sn—O-based oxide semiconductor, a Zn—O-based oxide semiconductor, or the like can be used.

In particular, an In—Ga—Zn—O-based oxide semiconductor material has sufficiently high resistance when there is no electrical field and thus the off-state current can be sufficiently reduced. In addition, the In—Ga—Zn—O-based oxide semiconductor material has high field-effect mobility and thus is suitable as a semiconductor material used for a semiconductor device.

As a typical example of the In—Ga—Zn—O-based oxide semiconductor material, the one represented by $InGaO_3(ZnO)_m$ (m>0) is given. In addition, there is an oxide semiconductor material in which Ga is replaced by M and which is represented by $InMO_3(ZnO)_m$ (m>0). Here, M denotes one or more metal elements selected from gallium (Ga), aluminum (Al), iron (Fe), nickel (Ni), manganese (Mn), cobalt (Co), and the like. For example, M can be Ga, Ga and Al, Ga and Fe, Ga and Ni, Ga and Mn, Ga and Co, or the like. Note that the above compositions are just examples obtained from a crystal structure.

It is preferable that a target having a composition expressed by the formula In:Ga:Zn=1:x:y (x is greater than or equal to 0, and y is greater than or equal to 0.5 and less than or equal to 5) be used as a target for forming the oxide semiconductor layer **144** by a sputtering method. For example, a target having a composition ratio of In:Ga:Zn=1:1:1 [atomic ratio] ($x=1$, $y=1$) (that is, $In_2O_3$:$Ga_2O_3$:$ZnO$=1:1:2 [molar ratio]) can be used. Alternatively, a target having a composition ratio of In:Ga:Zn=1:1:0.5 [atomic ratio] ($x=1$, $y=0.5$), a target having a composition ratio of In:Ga:Zn=1:1:2 [atomic ratio] ($x=1$, $y=2$), or a target having a composition ratio of In:Ga:Zn=1:0:1 [atomic ratio] ($x=0$, $y=1$) can be used.

In this embodiment, the oxide semiconductor layer **144** having an amorphous structure is formed by a sputtering method with the use of an In—Ga—Zn—O-based metal oxide target.

The relative density of the metal oxide in the metal oxide target is 80% or higher, preferably 95% or higher, more pref-

erably 99.9% or higher. With the use of the metal oxide target with high relative density, the oxide semiconductor layer **144** can be formed to have a dense structure.

The atmosphere in which the oxide semiconductor layer **144** is formed is preferably a rare gas (typically argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere including a rare gas (typically argon) and oxygen. Specifically, it is preferable to use, for example, an atmosphere of a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or hydride is removed so that the concentration is 1 ppm or lower (preferably the concentration is 10 ppb or lower).

In forming the oxide semiconductor layer **144**, for example, an object to be processed is held in a treatment chamber that is kept under reduced pressure and the object to be processed is heated so that the temperature of the object to be processed is higher than or equal to 100° C. and lower than 550° C., preferably higher than or equal to 200° C. and lower than or equal to 400° C. Alternatively, the temperature of the objected to be processed in the formation of the oxide semiconductor layer **144** may be room temperature. Then, moisture in the treatment chamber is removed, a sputtering gas from which hydrogen, water, and the like are removed is introduced, and the above target is used, so that the oxide semiconductor layer **144** is formed. By forming the oxide semiconductor layer **144** while heating the object to be processed, impurities in the oxide semiconductor layer **144** can be reduced. Further, damage due to sputtering can be reduced. In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, a titanium sublimation pump, or the like can be used. A turbo pump provided with a cold trap may be used. By performing evacuation with the use of a cryopump or the like, hydrogen, water, and the like can be removed from the treatment chamber; thus, the concentration of an impurity in the oxide semiconductor layer **144** can be reduced.

The oxide semiconductor layer **144** can be formed under the following conditions, for example: the distance between the object to be processed and the target is 170 mm, the pressure is 0.4 Pa, the direct current (DC) power is 0.5 kW, and the atmosphere is an oxygen (oxygen: 100%) atmosphere, an argon (argon: 100%) atmosphere, or a mixed atmosphere including oxygen and argon. Note that a pulsed direct current (DC) power source is preferable because dust (such as powder substances formed at the time of film formation) can be reduced and the film thickness can be uniform. The thickness of the oxide semiconductor layer **144** is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to 1 nm and less than or equal to 30 nm, more preferably greater than or equal to 1 nm and less than or equal to 10 nm. With the oxide semiconductor layer **144** having such a thickness, a short-channel effect which occurs along with miniaturization can be suppressed. Note that the appropriate thickness differs depending on the oxide semiconductor material to be used, the intended use of the semiconductor device, or the like; therefore, the thickness may be determined in accordance with the material, the intended use, or the like.

Note that before the oxide semiconductor layer **144** is formed by a sputtering method, a substance attached to a formation surface (e.g., a surface of the interlayer insulating layer **128**) is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. Here, the reverse sputtering is a method in which ions collide with a surface to be processed so that the surface is modified, in contrast to normal sputtering in which ions collide with a

sputtering target. An example of a method for making ions collide with a surface to be processed is a method in which high-frequency voltage is applied to the surface to be processed in an argon atmosphere so that plasma is generated in the vicinity of the object to be processed. Note that a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used instead of an argon atmosphere.

After that, heat treatment (first heat treatment) is preferably performed on the oxide semiconductor layer **144**. By the first heat treatment, excessive hydrogen (including water and a hydroxyl group) in the oxide semiconductor layer **144** can be removed, the structure of the oxide semiconductor layer can be modified, and defect levels in the energy gap can be reduced. The temperature of the first heat treatment is, for example, higher than or equal to 300° C. and lower than 550° C. or higher than or equal to 400° C. and lower than or equal to 500° C.

The heat treatment can be performed in such a manner that, for example, the object to be processed is introduced into an electric furnace in which a resistance heating element or the like is used and heated at 450° C. for one hour in a nitrogen atmosphere. During the heat treatment, the oxide semiconductor layer **144** is not exposed to air to prevent entry of water and hydrogen.

The heat treatment apparatus is not limited to the electric furnace and may be an apparatus for heating an object to be processed by thermal conduction or thermal radiation from a medium such as a heated gas. For example, a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. A GRTA apparatus is an apparatus for performing heat treatment using a high-temperature gas. As the gas, an inert gas that does not react with an object to be processed by heat treatment, for example, nitrogen or a rare gas such as argon is used.

For example, as the first heat treatment, GRTA treatment may be performed in the following manner. The object to be processed is put in an inert gas atmosphere that has been heated, heated for several minutes, and taken out of the inert gas atmosphere. GRTA treatment enables high-temperature heat treatment for a short time. Moreover, GRTA treatment can be employed even when the temperature exceeds the upper temperature limit of the object to be processed. Note that the inert gas may be switched to a gas including oxygen in the treatment. This is because defect levels in the energy gap due to oxygen deficiency can be reduced by performing the first heat treatment in an atmosphere including oxygen.

Note that as the inert gas atmosphere, an atmosphere that includes nitrogen or a rare gas (such as helium, neon, or argon) as a main component and does not include water, hydrogen, and the like is preferably used. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is higher than or equal to 6N (99.9999%), preferably higher than or equal to 7N (99.99999%) (that is, the concentration of an impurity is lower than or equal to 1 ppm, preferably lower than or equal to 0.1 ppm).

In any case, impurities are reduced by the first heat treatment so that the i-type (intrinsic) or substantially i-type oxide semiconductor layer **144** is obtained. Accordingly, a transistor having extremely excellent characteristics can be realized.

The above heat treatment (first heat treatment) has an effect of removing hydrogen, water, and the like and thus can be referred to as dehydration treatment, dehydrogenation treatment, or the like. The dehydration treatment or the dehydrogenation treatment can also be performed at the following timing: after the formation of the oxide semiconductor layer, after the formation of the gate insulating layer, after the formation of the gate electrode, or the like. Such dehydration treatment or dehydrogenation treatment may be performed once or plural times.

Next, the gate insulating layer 146 is formed in contact with the oxide semiconductor layer 144 (see FIG. 10C). The gate insulating layer 146 can be formed by a CVD method, a sputtering method, or the like. The gate insulating layer 146 is preferably formed so as to include silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, tantalum oxide, hafnium oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ (x>0, y>0)), hafnium silicate ($HfSi_xO_y$ (x>0, y>0)) to which nitrogen is added, hafnium aluminate ($HfAl_xO_y$ (x>0, y>0)) to which nitrogen is added, or the like. The gate insulating layer 146 may have a single-layer structure or a stacked structure. There is no particular limitation on the thickness of the gate insulating layer 146; in the case where the size of the semiconductor device is reduced, the gate insulating layer 146 is preferably thin in order to secure operation of the transistor. For example, in the case of using silicon oxide, the thickness can be greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

When the gate insulating layer is thin as in the above description, a problem of gate leakage due to a tunnel effect or the like is caused. In order to solve the problem of gate leakage, it is preferable that the gate insulating layer 146 be formed using a high dielectric constant (high-k) material such as hafnium oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ (x>0, y>0)), hafnium silicate ($HfSi_xO_y$ (x>0, y>0)) to which nitrogen is added, or hafnium aluminate ($HfAl_xO_y$ (x>0, y>0)) to which nitrogen is added. By using a high-k material for the gate insulating layer 146, the thickness thereof can be increased for suppression of gate leakage with favorable electric characteristics maintained. Note that a stacked structure of a film including a high-k material and a film including any of silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, and the like may also be employed.

After the gate insulating layer 146 is formed, second heat treatment is preferably performed in an inert gas atmosphere or an oxygen atmosphere. The temperature of the heat treatment is higher than or equal to 200° C. and lower than or equal to 450° C., preferably higher than or equal to 250° C. and lower than or equal to 350° C. For example, the heat treatment may be performed at 250° C. for one hour in a nitrogen atmosphere. The second heat treatment can reduce variation in electric characteristics of the transistor. Moreover, in the case where the gate insulating layer 146 includes oxygen, oxygen is supplied to the oxide semiconductor layer 144 to compensate for oxygen deficiency in the oxide semiconductor layer 144, whereby an i-type (intrinsic) or substantially i-type oxide semiconductor layer can be formed.

Note that the second heat treatment is performed after the gate insulating layer 146 is formed in this embodiment; however, the timing of the second heat treatment is not particularly limited to this. For example, the second heat treatment may be performed after the gate electrode is formed. Furthermore, the first heat treatment and the second heat treatment may be successively performed, the first heat treatment may

also serve as the second heat treatment, or the second heat treatment may also serve as the first heat treatment.

Next, over the gate insulating layer 146, the gate electrode 148a is formed in a region overlapping with the oxide semiconductor layer 144 and the electrode 148b is formed in a region overlapping with the source or drain electrode 142a (see FIG. 10D). The gate electrode 148a and the electrode 148b can be formed in such a manner that a conductive layer is formed over the gate insulating layer 146 and then etched selectively. The conductive layer to be the gate electrode 148a and the electrode 148b can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. The details are similar to those of the source or drain electrode 142a or the like; thus, description thereof can be referred to.

Next, the interlayer insulating layer 150 and the interlayer insulating layer 152 are formed over the gate insulating layer 146, the gate electrode 148a, and the electrode 148b (see FIG. 10E). The interlayer insulating layer 150 and the interlayer insulating layer 152 can be formed by a PVD method, a CVD method, or the like. The interlayer insulating layer 150 and the interlayer insulating layer 152 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, or tantalum oxide. Note that a stacked structure of the interlayer insulating layer 150 and the interlayer insulating layer 152 is employed in this embodiment; however, an embodiment of the disclosed invention is not limited to this. A single-layer structure or a stacked structure including three or more layers can also be employed. A structure in which an interlayer insulating layer is not provided may also be employed.

Note that the interlayer insulating layer 152 is preferably formed so as to have a planarized surface. By forming the interlayer insulating layer 152 so as to have a planarized surface, an electrode, a wiring, or the like can be favorably formed over the interlayer insulating layer 152 even in the case where the semiconductor device is reduced in size, for example. The interlayer insulating layer 152 can be planarized by a method such as chemical mechanical polishing (CMP) treatment.

Through the above steps, the transistor 162 including the purified oxide semiconductor layer 144 is completed (see FIG. 10E). The capacitor 164 is also completed.

The transistor 162 illustrated in FIG. 10E includes the oxide semiconductor layer 144; the source or drain electrode 142a and the source or drain electrode 142b which are electrically connected to the oxide semiconductor layer 144; the gate insulating layer 146 which covers the oxide semiconductor layer 144, the source or drain electrode 142a, and the source or drain electrode 142b; and the gate electrode 148a over the gate insulating layer 146. Further, the capacitor 164 includes the source or drain electrode 142a, the oxide semiconductor layer 144, the gate insulating layer 146 which covers the source or drain electrode 142a, and the electrode 148b over the gate insulating layer 146.

In the transistor 162 described in this embodiment, the oxide semiconductor layer 144 is purified and thus the hydrogen concentration thereof is lower than or equal to $5 \times 10^{19}$ atoms/cm$^3$, preferably lower than or equal to $5 \times 10^{18}$ atoms/cm$^3$, more preferably lower than or equal to $5 \times 10^{17}$ atoms/cm$^3$. The carrier density of the oxide semiconductor layer 144 is sufficiently low (e.g., lower than $1 \times 10^{12}$/cm$^3$, preferably lower than $1.45 \times 10^{10}$/cm$^3$) as compared to the carrier density of a general silicon wafer (approximately $1 \times 10^{14}$/cm$^3$). Accordingly, the off-state current is sufficiently small. For example, the off-state current (here, current per micrometer

of channel width) of the transistor **162** at room temperature is less than or equal to 100 zA/μm (1 zA (zeptoampere) is $1\times10^{-21}$ A), preferably less than or equal to 10 zA/μm.

With the use of the purified and intrinsic oxide semiconductor layer **144**, the off-state current of a transistor can be sufficiently reduced. Further, with the use of such a transistor, a semiconductor device capable of retaining stored data for an extremely long time can be obtained.

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

### Embodiment 5

In this embodiment, a structure and a manufacturing method of a semiconductor device according to an embodiment of the disclosed invention, which are different from those of Embodiment 4, will be described with reference to FIGS. **11A** and **11B**, FIGS. **12A** to **12D**, and FIGS. **13A** and **13B**.

<Cross-Sectional Structure and Planar Structure of Semiconductor Device>

FIGS. **11A** and **11B** illustrate an example of a structure of a semiconductor device. FIG. **11A** illustrates a cross section of the semiconductor device, and FIG. **11B** illustrates a plan view of the semiconductor device. Here, FIG. **11A** corresponds to a cross section along line A3-A4 and line B3-B4 in FIG. **11B**. The semiconductor device illustrated in FIGS. **11A** and **11B** includes the transistor **160** including a material other than an oxide semiconductor in a lower portion, and the transistor **162** including an oxide semiconductor in an upper portion. A transistor including a material other than an oxide semiconductor can operate at high speed easily. On the other hand, a transistor including an oxide semiconductor can hold electric charge for a long time owing to its characteristics.

Although both of the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. Since the technical nature of the disclosed invention is to use an oxide semiconductor in the transistor **162** so that data can be stored, it is not necessary to limit a specific structure of a semiconductor device to the structure described here.

The transistor **160** in FIGS. **11A** and **11B** includes the channel formation region **116** provided in the substrate **100** including a semiconductor material (e.g., silicon), the impurity regions **114** and the high-concentration impurity regions **120** (these regions are also collectively referred to simply as impurity regions) provided so that the channel formation region **116** is sandwiched therebetween, the gate insulating layer **108** provided over the channel formation region **116**, the gate electrode **110** provided over the gate insulating layer **108**, and the source or drain electrode **130a** and the source or drain electrode **130b** electrically connected to the impurity regions. Further, a wiring **142c** and a wiring **142d** are provided over the source or drain electrode **130a** and the source or drain electrode **130b**. Note that as the semiconductor material, for example, silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like can be used, and a single crystal semiconductor is preferably used.

The sidewall insulating layer **118** is provided on a side surface of the gate electrode **110**. The high-concentration impurity region **120** is positioned in a region of the substrate **100**, which does not overlap with the sidewall insulating layer **118** when seen from a direction perpendicular to the surface of the substrate **100**. The metal compound region **124** is positioned in contact with the high-concentration impurity

region **120**. The element isolation insulating layer **106** is provided over the substrate **100** so as to surround the transistor **160**. The interlayer insulating layer **126** and the interlayer insulating layer **128** are provided so as to cover the transistor **160**. The source or drain electrode **130a** and the source or drain electrode **130b** are electrically connected to the metal compound regions **124** through openings formed in the interlayer insulating layer **126**. That is, each of the source or drain electrode **130a** and the source or drain electrode **130b** is electrically connected to the high-concentration impurity region **120** and the impurity region **114** through the metal compound region **124**. Note that the sidewall insulating layer **118** is not formed in some cases for integration of the transistor **160** or the like.

The transistor **162** in FIGS. **11A** and **11B** includes the source or drain electrode **142a** and the source or drain electrode **142b** which are provided over the interlayer insulating layer **128**; the island-shaped oxide semiconductor layer **144** which is electrically connected to the source or drain electrode **142a** and the source or drain electrode **142b**; the gate insulating layer **146** which covers the source or drain electrode **142a**, the source or drain electrode **142b**, and the island-shaped oxide semiconductor layer **144**; and the gate electrode **148a** which is provided over the gate insulating layer **146** so as to overlap with the island-shaped oxide semiconductor layer **144**.

Here, the source or drain electrode **142a** is formed on and in direct contact with the gate electrode **110**, whereby the transistor **160** in the lower portion and the transistor **162** in the upper portion are electrically connected to each other. That is, the semiconductor device described in this embodiment has a structure in which the transistor **162** in the upper portion is formed above the transistor **160** in the lower portion, from which a portion over the top surface of the gate electrode **110** is removed, in the semiconductor device described in Embodiment 4.

Note that it is preferable that the oxide semiconductor layer **144** be purified by sufficient removal of impurities such as hydrogen or sufficient supply of oxygen. Specifically, the concentration of hydrogen in the oxide semiconductor layer **144** is lower than or equal to $5\times10^{19}$ atoms/cm$^3$, preferably lower than or equal to $5\times10^{18}$ atoms/cm$^3$, more preferably lower than or equal to $5\times10^{17}$ atoms/cm$^3$, for example. Note that the concentration of hydrogen in the oxide semiconductor layer **144** is measured by secondary ion mass spectrometry (SIMS). Thus, in the oxide semiconductor layer **144** in which the hydrogen concentration is sufficiently reduced so that the oxide semiconductor layer is purified and defect levels in the energy gap due to oxygen deficiency are reduced by sufficient supply of oxygen, the carrier density is lower than $1\times10^{12}$/cm$^3$, preferably lower than $1\times10^{11}$/cm$^3$, more preferably lower than $1.45\times10^{10}$/cm$^3$. For example, the off-state current (here, current per micrometer of channel width) at room temperature is less than or equal to 100 zA/μm (1 zA (zeptoampere) is $1\times10^{-21}$ A), preferably less than or equal to 10 zA/μm. With the use of such an i-type (intrinsic) or substantially i-type oxide semiconductor, the transistor **162** which has extremely excellent off-current characteristics can be obtained.

The capacitor **164** includes the source or drain electrode **142a**, the oxide semiconductor layer **144**, the gate insulating layer **146**, and the electrode **148b**. That is, the source or drain electrode **142a** functions as one electrode of the capacitor **164**, and the electrode **148b** functions as the other electrode of the capacitor **164**.

Note that in the capacitor **164** in FIGS. **11A** and **11B**, the oxide semiconductor layer **144** and the gate insulating layer

**146** are stacked, whereby insulation between the source or drain electrode **142a** and the electrode **148b** can be sufficiently secured.

Note that in the transistor **162** and the capacitor **164**, end portions of the source or drain electrode **142a** and the source or drain electrode **142b** are preferably tapered. Here, the taper angle is greater than or equal to 30° and less than or equal to 60°, for example. Note that the taper angle is a tilt angle formed by a side surface and a bottom surface of a layer having a tapered shape (e.g., the source or drain electrode **142a**) in the case where the layer is observed from a direction perpendicular to a cross section (a plane perpendicular to the surface of a substrate). The end portions of the source or drain electrode **142a** and the source or drain electrode **142b** are tapered, whereby coverage with the oxide semiconductor layer **144** can be improved and disconnection can be prevented.

Further, the interlayer insulating layer **150** is provided over the transistor **162** and the capacitor **164**, and the interlayer insulating layer **152** is provided over the interlayer insulating layer **150**.

<Method for Manufacturing Semiconductor Device>

Next, an example of a method for manufacturing the semiconductor device will be described. Hereinafter, steps performed after formation of the transistor **160** in the lower portion and a method for manufacturing the transistor **162** in the upper portion will be described with reference to FIGS. **12A** to **12D**. The transistor **160** in the lower portion can be manufactured by a method similar to that described in Embodiment 4, and description in Embodiment 4 can be referred to.

The transistor **160** in the lower portion is formed by the method described in Embodiment 4 first, and then a portion of the transistor **160** over the top surface of the gate electrode **110** is removed (see FIG. **12A**). The portion of the transistor **160** over the top surface of the gate electrode **110** is removed by performing polishing treatment (e.g., CMP treatment) on the transistor **160** in the lower portion until the top surface of the gate electrode **110** is exposed. Thus, portions of the interlayer insulating layers **126** and **128** and the source and drain electrodes **130a** and **130b** over the gate electrode **110** are removed by the CMP treatment. At this time, the surface including the interlayer insulating layers **126** and **128** and the source and drain electrodes **130a** and **130b** is planarized, so that an electrode, a wiring, an insulating layer, a semiconductor layer, and the like can be favorably formed in later steps. In addition, the electrode **130c** described in Embodiment 4 would be completely removed by the CMP treatment and thus does not need to be formed.

The top surface of the gate electrode **110** is exposed by the CMP treatment in this manner, whereby the gate electrode **110** and the source or drain electrode **142a** can be in direct contact with each other; accordingly, the transistor **160** and the transistor **162** can be easily electrically connected to each other.

Next, a conductive layer is formed over the interlayer insulating layers **126** and **128** and etched selectively, so that the source or drain electrode **142a**, the source or drain electrode **142b**, the wiring **142c**, and the wiring **142d** are formed (see FIG. **12B**). Here, the source or drain electrode **142a**, the wiring **142c**, and the wiring **142d** are formed so as to be in direct contact with the gate electrode **110**, the source or drain electrode **130a**, and the source or drain electrode **130b**, respectively.

Here, for the conductive layer used for forming the source or drain electrode **142a**, the source or drain electrode **142b**, the wiring **142c**, and the wiring **142d**, a material similar to that

described in Embodiment 4 can be used and description in Embodiment 4 can be referred to. Etching of the conductive layer can also be performed in a manner similar to the method described in Embodiment 4, and description in Embodiment 4 can be referred to.

Further, as in the case of Embodiment 4, an insulating layer may be formed over the source or drain electrode **142a** and the source or drain electrode **142b**. By providing the insulating layer, parasitic capacitance between a gate electrode formed later and the source and drain electrodes **142a** and **142b** can be reduced.

Next, an oxide semiconductor layer is formed so as to cover the source or drain electrode **142a**, the source or drain electrode **142b**, the wiring **142c**, and the wiring **142d** and the oxide semiconductor layer is selectively etched, so that the oxide semiconductor layer **144** is formed in contact with the source or drain electrode **142a** and the source or drain electrode **142b** (see FIG. **12C**).

The oxide semiconductor layer can be formed using a material and a method similar to those described in Embodiment 4. Therefore, Embodiment 4 can be referred to for a material and a formation method of the oxide semiconductor layer.

The oxide semiconductor layer formed in this manner is processed into an island shape by a method such as etching using a mask, so that the island-shaped oxide semiconductor layer **144** is formed.

As the etching of the oxide semiconductor layer, either dry etching or wet etching may be employed. Needless to say, dry etching and wet etching can be used in combination. The etching conditions (such as an etching gas, an etchant, etching time, and temperature) are set as appropriate in accordance with the material so that the oxide semiconductor layer can be etched into a desired shape.

Further, the oxide semiconductor layer **144** is preferably subjected to heat treatment (first heat treatment) in a manner similar to that described in Embodiment 4. The first heat treatment can be performed by the method described in Embodiment 4, and Embodiment 4 can be referred to. Impurities are reduced by the first heat treatment so that the i-type (intrinsic) or substantially i-type oxide semiconductor layer **144** is obtained. Accordingly, a transistor having extremely excellent characteristics can be realized. Note that the first heat treatment may be performed before the oxide semiconductor layer is etched or after the oxide semiconductor layer is etched to be processed into an island shape.

Next, the gate insulating layer **146** is formed in contact with the oxide semiconductor layer **144** (see FIG. **12C**).

The gate insulating layer **146** can be formed using a material and a method similar to those described in Embodiment 4. Therefore, Embodiment 4 can be referred to for a material and a formation method of the gate insulating layer **146**.

After the gate insulating layer **146** is formed, second heat treatment is preferably performed in an inert gas atmosphere or an oxygen atmosphere in a manner similar to that described in Embodiment 4. The second heat treatment can be performed by the method described in Embodiment 4, and Embodiment 4 can be referred to. The second heat treatment can reduce variation in electric characteristics of the transistor. Moreover, in the case where the gate insulating layer **146** includes oxygen, oxygen is supplied to the oxide semiconductor layer **144** to compensate for oxygen deficiency in the oxide semiconductor layer **144**, whereby an i-type (intrinsic) or substantially i-type oxide semiconductor layer can be formed.

Note that the second heat treatment is performed after the gate insulating layer **146** is formed in this embodiment; how-

ever, the timing of the second heat treatment is not particularly limited to this. For example, the second heat treatment may be performed after the gate electrode is formed. Furthermore, the first heat treatment and the second heat treatment may be successively performed, the first heat treatment may also serve as the second heat treatment, or the second heat treatment may also serve as the first heat treatment.

Next, over the gate insulating layer 146, the gate electrode 148a is formed in a region overlapping with the oxide semiconductor layer 144 and the electrode 148b is formed in a region overlapping with the source or drain electrode 142a (see FIG. 12D). The gate electrode 148a and the electrode 148b can be formed in such a manner that a conductive layer is formed over the gate insulating layer 146 and then etched selectively. The conductive layer to be the gate electrode 148a and the electrode 148b can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. The details are similar to those of the source or drain electrode 142a or the like; thus, description thereof can be referred to.

Next, in a manner similar to that described in Embodiment 4, the interlayer insulating layer 150 and the interlayer insulating layer 152 are formed over the gate insulating layer 146, the gate electrode 148a, and the electrode 148b. The interlayer insulating layer 150 and the interlayer insulating layer 152 can be formed using materials and methods similar to those described in Embodiment 4. Therefore, Embodiment 4 can be referred to for materials and formation methods of the interlayer insulating layer 150 and the interlayer insulating layer 152.

Note that the interlayer insulating layer 152 is preferably formed so as to have a planarized surface. By forming the interlayer insulating layer 152 so as to have a planarized surface, an electrode, a wiring, or the like can be favorably formed over the interlayer insulating layer 152 even in the case where the semiconductor device is reduced in size, for example. The interlayer insulating layer 152 can be planarized by a method such as chemical mechanical polishing (CMP) treatment.

Through the above steps, the transistor 162 including the purified oxide semiconductor layer 144 is completed (see FIGS. 12A to 12D). The capacitor 164 is also completed.

The transistor 162 illustrated in FIG. 12D includes the oxide semiconductor layer 144; the source or drain electrode 142a and the source or drain electrode 142b which are electrically connected to the oxide semiconductor layer 144; the gate insulating layer 146 which covers the oxide semiconductor layer 144, the source or drain electrode 142a, and the source or drain electrode 142b; and the gate electrode 148a over the gate insulating layer 146. Further, the capacitor 164 includes the source or drain electrode 142a, the oxide semiconductor layer 144, the gate insulating layer 146 which covers the source or drain electrode 142a, and the electrode 148b over the gate insulating layer 146.

<Cross-Sectional View and Plan View of Semiconductor Device>

Next, a structure of a semiconductor device according to an embodiment of the disclosed invention, which is different from that in FIGS. 11A and 11B, and a manufacturing method thereof will be described with reference to FIGS. 23A and 23B and FIGS. 24A to 24D.

FIGS. 23A and 23B illustrate an example of a structure of a semiconductor device. FIG. 23A illustrates a cross section of the semiconductor device, and FIG. 23B illustrates a plan view of the semiconductor device. Here, FIG. 23A corresponds to a cross section along line E1-E2 and line F1-F2 in FIG. 23B. The semiconductor device illustrated in FIGS. 23A and 23B includes the transistor 160 including a material other than an oxide semiconductor in a lower portion, and a transistor 163 including an oxide semiconductor in an upper portion. The structure of the transistor 160 in the lower portion in FIGS. 23A and 23B is similar to that in FIGS. 11A and 11B and thus is not described in detail.

The oxide semiconductor layer 144, the source or drain electrode 142a, the source or drain electrode 142b, the gate insulating layer 146, and the gate electrode 148a are included in both the transistor 163 illustrated in FIGS. 23A and 23B and the transistor 162 illustrated in FIGS. 11A and 11B. A difference between the transistor 163 and the transistor 162 is positions where the oxide semiconductor layer 144 is in contact with the source or drain electrode 142a and the source or drain electrode 142b. That is, in the transistor 163, upper portions of the oxide semiconductor layer 144 are in contact with the source or drain electrode 142a and the source or drain electrode 142b.

In FIGS. 23A and 23B, the oxide semiconductor layer 144 can have a uniform thickness by improving the planarity of the interlayer insulating layer 128 over which the oxide semiconductor layer 144 is formed; thus, the characteristics of the transistor 163 can be improved.

The source or drain electrode 142a, the gate insulating layer 146, and the electrode 148b are included in both a capacitor 165 illustrated in FIGS. 23A and 23B and the capacitor 164 illustrated in FIGS. 11A and 11B. A difference between the capacitor 165 and the capacitor 164 is that the capacitor 165 does not include the oxide semiconductor layer 144.

The capacitor 165 does not include the oxide semiconductor layer 144, whereby the capacitor 165 can have larger capacitance than the capacitor 164 in the case where the gate insulating layer 146 of the transistor 162 is formed using the same material and has the same thickness as the gate insulating layer 146 of the transistor 163.

Further, the interlayer insulating layer 150 is provided over the transistor 163 and the capacitor 165, and the interlayer insulating layer 152 is provided over the interlayer insulating layer 150.

<Method for Manufacturing Semiconductor Device>

Next, an example of a method for manufacturing the semiconductor device will be described. Hereinafter, a method for manufacturing the transistor 163 in the upper portion after formation of the transistor 160 in the lower portion will be described with reference to FIGS. 24A to 24D. The transistor in the lower portion can be manufactured by a method similar to that described in Embodiment 4, and description in Embodiment 4 can be referred to.

The transistor 160 in the lower portion is formed by the method described in Embodiment 4 first, and then a portion of the transistor 160 over a top surface of the gate electrode 110 is removed (see FIG. 24A). The portion of the transistor 160 over the top surface of the gate electrode 110 is removed by performing CMP treatment on the transistor 160 in the lower portion until the top surface of the gate electrode 110 is exposed. Thus, portions of the interlayer insulating layers 126 and 128 and the source and drain electrodes 130a and 130b over the gate electrode 110 are removed by the CMP treatment. At this time, by planarizing surfaces of the interlayer insulating layers 126 and 128 and the source and drain electrodes 130a and 130b over which an oxide semiconductor layer is formed later, the oxide semiconductor layer 144 can have a uniform thickness.

Next, an oxide semiconductor layer is formed over the interlayer insulating layers 126 and 128 and the source and drain electrodes 130a and 130b, which are planarized, and the

oxide semiconductor layer is selectively etched, so that the oxide semiconductor layer **144** is formed (see FIG. **24**A).

The oxide semiconductor layer can be formed using a material and a method similar to those described in Embodiment 4. Therefore, Embodiment 4 may be referred to for a material and a formation method of the oxide semiconductor layer.

The oxide semiconductor layer formed in this manner is processed into an island shape by a method such as etching using a mask, so that the island-shaped oxide semiconductor layer **144** is formed. Embodiment 4 may be referred to for a method for processing the oxide semiconductor layer.

Further, the oxide semiconductor layer **144** is preferably subjected to heat treatment (first heat treatment) in a manner similar to that described in Embodiment 4. The first heat treatment can be performed by the method described in Embodiment 4, and Embodiment 4 can be referred to. Impurities are reduced by the first heat treatment so that the i-type (intrinsic) or substantially i-type oxide semiconductor layer **144** is obtained. Accordingly, a transistor having extremely excellent characteristics can be realized. Note that the first heat treatment may be performed before the oxide semiconductor layer is etched or after the oxide semiconductor layer is etched to be processed into an island shape.

Next, a conductive layer is formed over the oxide semiconductor layer **144** and the like and etched selectively, so that the source or drain electrode **142***a*, the source or drain electrode **142***b*, and the wirings **142***c* and **142***d* are formed (see FIG. **24**B). Here, the source or drain electrode **142***a*, the wiring **142***c*, and the wiring **142***d* are formed so as to be in direct contact with the gate electrode **110**, the source or drain electrode **130***a*, and the source or drain electrode **130***b*, respectively.

Here, for the conductive layer used for forming the source or drain electrode **142***a*, the source or drain electrode **142***b*, the wiring **142***c*, and the wiring **142***d*, a material similar to that described in Embodiment 4 can be used and description in Embodiment 4 can be referred to. Etching of the conductive layer can also be performed in a manner similar to the method described in Embodiment 4, and description in Embodiment 4 can be referred to.

In the above manner, the top surface of the gate electrode **110** is exposed by removing portions of the interlayer insulating layers **126** and **128** over the gate electrode **110** by CMP treatment, whereby the gate electrode **110** and the source or drain electrode **142***a* can be in direct contact with each other; accordingly, the transistor **160** and the transistor **163** can be easily electrically connected to each other.

Next, the gate insulating layer **146** is formed in contact with the oxide semiconductor layer **144** (see FIG. **24**C).

The gate insulating layer **146** can be formed using a material and a method similar to those described in Embodiment 4. Therefore, Embodiment 4 can be referred to for a material and a formation method of the gate insulating layer **146**.

After the gate insulating layer **146** is formed, second heat treatment is preferably performed in an inert gas atmosphere or an oxygen atmosphere in a manner similar to that described in Embodiment 4. The second heat treatment can be performed by the method described in Embodiment 4, and Embodiment 4 can be referred to. The second heat treatment can reduce variation in electric characteristics of the transistors. Moreover, in the case where the gate insulating layer **146** includes oxygen, oxygen is supplied to the oxide semiconductor layer **144** to compensate for oxygen deficiency in the oxide semiconductor layer **144**, whereby an i-type (intrinsic) or substantially i-type oxide semiconductor layer can be formed.

Note that the second heat treatment is performed after the gate insulating layer **146** is formed in this embodiment; however, the timing of the second heat treatment is not particularly limited to this. For example, the second heat treatment may be performed after the gate electrode **148***a* is formed. Furthermore, the first heat treatment and the second heat treatment may be successively performed, the first heat treatment may also serve as the second heat treatment, or the second heat treatment may also serve as the first heat treatment.

Next, over the gate insulating layer **146**, the gate electrode **148***a* is formed in a region overlapping with the oxide semiconductor layer **144** and the electrode **148***b* is formed in a region overlapping with the source or drain electrode **142***a* (see FIG. **24**C). The gate electrode **148***a* and the electrode **148***b* can be formed in such a manner that a conductive layer is formed over the gate insulating layer **146** and then etched selectively. The conductive layer to be the gate electrode **148***a* and the electrode **148***b* can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. The details are similar to those of the source or drain electrode **142***a* or the like; thus, description thereof can be referred to.

Next, in a manner similar to that described in Embodiment 4, the interlayer insulating layer **150** and the interlayer insulating layer **152** are formed over the gate insulating layer **146**, the gate electrode **148***a*, and the electrode **148***b*. The interlayer insulating layer **150** and the interlayer insulating layer **152** can be formed using materials and methods similar to those described in Embodiment 4. Therefore, Embodiment 4 can be referred to for materials and formation methods of the interlayer insulating layer **150** and the interlayer insulating layer **152**.

Note that the interlayer insulating layer **152** is preferably formed so as to have a planarized surface. By forming the interlayer insulating layer **152** so as to have a planarized surface, an electrode, a wiring, or the like can be favorably formed over the interlayer insulating layer **152** even in the case where the semiconductor device is reduced in size, for example. The interlayer insulating layer **152** can be planarized by a method such as chemical mechanical polishing (CMP) treatment.

Through the above steps, the transistor **163** including the purified oxide semiconductor layer **144** is completed (see FIG. **24**D). The capacitor **165** is also completed.

The transistor **163** illustrated in FIG. **24**D includes the oxide semiconductor layer **144**; the source and drain electrodes **142***a* and **142***b* which are electrically connected to the oxide semiconductor layer **144**; the gate insulating layer **146** which covers the oxide semiconductor layer **144** and the source and drain electrodes **142***a* and **142***b*; and the gate electrode **148***a* over the gate insulating layer **146**. Further, the capacitor **165** illustrated in FIG. **24**D includes the source or drain electrode **142***a*, the gate insulating layer **146**, and the electrode **148***b* over the gate insulating layer **146**.

In the transistor **162** and the transistor **163** described in this embodiment, the oxide semiconductor layer **144** is purified and thus the hydrogen concentration thereof is lower than or equal to $5 \times 10^{19}$ atoms/cm$^3$, preferably lower than or equal to $5 \times 10^{18}$ atoms/cm$^3$, more preferably lower than or equal to $5 \times 10^{17}$ atoms/cm$^3$. The carrier density of the oxide semiconductor layer **144** is sufficiently low (e.g., lower than $1 \times 10^{12}$/cm$^3$, preferably lower than $1.45 \times 10^{10}$/cm$^3$) as compared to the carrier density of a general silicon wafer (approximately $1 \times 10^{14}$/cm$^3$). Accordingly, the off-state current is sufficiently small. For example, the off-state current (here, current per micrometer of channel width) of each of the transistor **162**

and the transistor **163** at room temperature is less than or equal to 100 zA/m (1 zA (zeptoampere) is $1\times10^{-21}$ A), preferably less than or equal to 10 zA/μm.

With the use of the purified and intrinsic oxide semiconductor layer **144**, the off-state current of a transistor can be sufficiently reduced. Further, with the use of such a transistor, a semiconductor device capable of retaining stored data for an extremely long time can be obtained.

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

Embodiment 6

In this embodiment, a structure and a manufacturing method of a semiconductor device according to an embodiment of the disclosed invention, which are different from those of Embodiments 4 and 5, will be described with reference to FIGS. **13**A and **13**B, FIGS. **14**A to **14**D, and FIGS. **15**A to **15**C.

<Cross-Sectional Structure and Planar Structure of Semiconductor Device>

FIGS. **13**A and **13**B illustrate an example of a structure of a semiconductor device. FIG. **13**A illustrates a cross section of the semiconductor device, and FIG. **13**B illustrates a plan view of the semiconductor device. Here, FIG. **13**A corresponds to a cross section along line **C1**-**C2** and line **D 1**-**D2** in FIG. **13**B. In the plan view of FIG. **13**B, some of components, such as a source or drain electrode **154** and a wiring **156**, are omitted to avoid complexity. The semiconductor device illustrated in FIGS. **13**A and **13**B includes the transistor **160** including a semiconductor material other than an oxide semiconductor in a lower portion, and the transistor **162** including an oxide semiconductor in an upper portion. A transistor including a semiconductor material other than an oxide semiconductor can operate at high speed easily. On the other hand, a transistor including an oxide semiconductor can hold electric charge for a long time owing to its characteristics.

Although both of the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. Since the technical nature of the disclosed invention is to use an oxide semiconductor in the transistor **162** so that data can be stored, it is not necessary to limit a specific structure of a semiconductor device to the structure described here.

The semiconductor device in FIGS. **13**A and **13**B is different from the semiconductor devices described in the above embodiments in a planar layout of the semiconductor device. In this embodiment, the transistor **162** and the capacitor **164** are provided so as to overlap with the transistor **160**. By employing such a planar layout, high integration is possible. For example, given that the minimum processing dimension is F, the area occupied by a memory cell can be 15 $F^2$ to 25 $F^2$.

The semiconductor device in FIGS. **13**A and **13**B is different from the semiconductor devices described in the above embodiments also in that the sidewall insulating layer **118** is not provided in the transistor **160**. That is, the semiconductor device in FIGS. **13**A and **13**B does not include a sidewall insulating layer. Since a sidewall insulating layer is not formed, the impurity region **114** is not formed. Thus, in the case where the sidewall insulating layer is not provided, high integration is easy as compared to the case where the sidewall insulating layer **118** is provided. In addition, the manufacturing process can be simplified as compared to the case where the sidewall insulating layer **118** is provided.

The semiconductor device in FIGS. **13**A and **13**B is different from the semiconductor devices described in the above embodiments also in that an interlayer insulating layer **125** is provided in the transistor **160**. That is, the semiconductor device in FIGS. **13**A and **13**B includes the interlayer insulating layer **125**. By using an insulating layer including hydrogen as the interlayer insulating layer **125**, hydrogen can be supplied to the transistor **160** and the characteristics of the transistor **160** can be improved. As the interlayer insulating layer **125**, for example, a silicon nitride layer including hydrogen, which is formed by a plasma CVD method, is given. Further, by using an insulating layer in which hydrogen is sufficiently reduced as the interlayer insulating layer **126**, hydrogen which might adversely affect the characteristics of the transistor **162** can be prevented from being included in the transistor **162**. As the interlayer insulating layer **126**, for example, a silicon nitride layer formed by a sputtering method is given. When such a structure is employed, the characteristics of the transistor **160** and the transistor **162** can be improved sufficiently.

The semiconductor device in FIGS. **13**A and **13**B is different from the semiconductor devices described in the above embodiments also in that an insulating layer **143***a* and an insulating layer **143***b* are provided in the transistor **162**. That is, the semiconductor device in FIGS. **13**A and **13**B includes the insulating layer **143***a* and the insulating layer **143***b*. By thus providing the insulating layer **143***a* and the insulating layer **143***b*, so-called gate capacitance formed by the gate electrode **148***a* and the source or drain electrode **142***a* (or the gate electrode **148***a* and the source or drain electrode **142***b*) can be reduced and the operation speed of the transistor **162** can be increased.

Furthermore, the semiconductor device in FIGS. **13**A and **13**B is different from the semiconductor devices described in the above embodiments also in that the source or drain electrode **154** of the transistor **160** is provided in contact with the wiring **156**.

Note that as in Embodiment 5, the source or drain electrode **142***a* is formed directly on the gate electrode **110**, whereby the transistor **160** in the lower portion and the transistor **162** in the upper portion are electrically connected to each other. With such a structure, the integration degree is increased as compared to the case where an electrode or a wiring are provided additionally. In addition, the manufacturing process is simplified.

Although the structure including all the differences is described in this embodiment, a structure including any one of the differences may be employed.

<Method for Manufacturing Semiconductor Device>

Next, an example of a method for manufacturing the semiconductor device will be described. Hereinafter, steps performed after formation of the transistor **160** in the lower portion and a method for manufacturing the transistor **162** in the upper portion will be described with reference to FIGS. **14**A to **14**D and FIGS. **15**A to **15**C. The transistor **160** in the lower portion can be manufactured by a method similar to that described in Embodiment 4. Embodiment 4 can be referred to for the details. Note that the three interlayer insulating layers **125**, **126**, and **128** are formed so as to cover the transistor **160** in this embodiment (cf. FIG. **9**G). In addition, the source or drain electrode **130***a* and the source or drain electrode **130***b* are not formed in the manufacturing process of the transistor **160** in this embodiment (cf. FIG. **9**H); however, even the structure in which the source or drain electrode **130***a* and the source or drain electrode **130***b* are not formed is called the transistor **160** for convenience.

The transistor 160 in the lower portion is formed by the method described in Embodiment 4 first, and then a portion of the transistor 160 over a top surface of the gate electrode 110 is removed. For the removing step, polishing treatment such as chemical mechanical polishing (CMP) treatment may be used. Thus, portions of the interlayer insulating layer 125, the interlayer insulating layer 126, and the interlayer insulating layer 128 over the top surface of the gate electrode 110 are removed. Note that the surface subjected to polishing treatment is planarized sufficiently, whereby an electrode, a wiring, an insulating layer, a semiconductor layer, and the like can be favorably formed in later steps.

Then, a conductive layer is formed over the gate electrode 110, the interlayer insulating layer 125, the interlayer insulating layer 126, and the interlayer insulating layer 128, and the conductive layer is etched selectively, so that the source or drain electrode 142a and the source or drain electrode 142b are formed (see FIG. 14A). Here, the source or drain electrode 142a is formed so as to be in direct contact with the gate electrode 110.

The conductive layer used for forming the source or drain electrode 142a and the source or drain electrode 142b can be formed using a material similar to that described in Embodiment 4. Further, the conductive layer can be etched by a method similar to that described in Embodiment 4. Embodiment 4 can be referred to for the details.

Next, an insulating layer is formed so as to cover the source or drain electrode 142a and the source or drain electrode 142b and etched selectively, so that the insulating layer 143a and the insulating layer 143b are formed over the source or drain electrode 142a and the source or drain electrode 142b, respectively (see FIG. 14B).

By providing the insulating layer 143a and the insulating layer 143b, parasitic capacitance between a gate electrode formed later and the source and drain electrodes 142a and 142b can be reduced.

After that, the oxide semiconductor layer 144 is formed so as to cover the source or drain electrode 142a and the source or drain electrode 142b, and the gate insulating layer 146 is formed over the oxide semiconductor layer 144 (see FIG. 14C).

The oxide semiconductor layer 144 can be formed using the material and the method described in Embodiment 4. Further, the oxide semiconductor layer 144 is preferably subjected to heat treatment (first heat treatment). Embodiment 4 can be referred to for the details.

The gate insulating layer 146 can be formed using the material and the method described in Embodiment 4. After the gate insulating layer 146 is formed, heat treatment (second heat treatment) is preferably performed in an inert gas atmosphere or an oxygen atmosphere. Embodiment 4 can be referred to for the details.

Then, over the gate insulating layer 146, the gate electrode 148a is formed in a region overlapping with a region of the transistor 162, which serves as a channel formation region, and the electrode 148b is formed in a region overlapping with the source or drain electrode 142a (see FIG. 14D).

The gate electrode 148a and the electrode 148b can be formed in such a manner that a conductive layer is formed over the gate insulating layer 146 and then etched selectively. The conductive layer to be the gate electrode 148a and the electrode 148b can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. The details are similar to those of the source or drain electrode 142a or the like; thus, the description thereof can be referred to.

Next, the interlayer insulating layer 150 and the interlayer insulating layer 152 are formed over the gate insulating layer 146, the gate electrode 148a, and the electrode 148b (see FIG. 15A). The interlayer insulating layer 150 and the interlayer insulating layer 152 can be formed using the materials and the methods described in Embodiment 4. Embodiment 4 can be referred to for the details.

Note that the interlayer insulating layer 152 is preferably formed so as to have a planarized surface. By forming the interlayer insulating layer 152 so as to have a planarized surface, an electrode, a wiring, or the like can be favorably formed over the interlayer insulating layer 152 even in the case where the semiconductor device is reduced in size, for example. The interlayer insulating layer 152 can be planarized by a method such as chemical mechanical polishing (CMP) treatment.

After that, the interlayer insulating layer 125, the interlayer insulating layer 126, the interlayer insulating layer 128, the oxide semiconductor layer 144, the gate insulating layer 146, the interlayer insulating layer 150, and the interlayer insulating layer 152 are selectively etched, so that an opening that reaches the metal compound region 124 of the transistor 160 is formed (see FIG. 15B). As the etching, either dry etching or wet etching may be used; in terms of microfabrication, dry etching is preferably used.

The source or drain electrode 154 is formed so as to be embedded in the opening. Then, the wiring 156 is formed to be connected to the source or drain electrode 154 (see FIG. 15C).

The source or drain electrode 154 can be formed in such a manner, for example, that a conductive layer is formed in a region including the opening by a PVD method, a CVD method, or the like and then part of the conductive layer is removed by etching treatment, CMP treatment, or the like. Specifically, it is possible to employ a method, for example, in which a thin titanium film is formed in a region including the opening by a PVD method, a thin titanium nitride film is formed by a CVD method, and then a tungsten film is formed so as to be embedded in the opening. Here, the titanium film formed by a PVD method has a function of reducing an oxide film (such as a natural oxide film) formed on a surface over which the titanium film is formed, thereby lowering the contact resistance with a lower electrode or the like (the metal compound region 124, here). The titanium nitride film formed after the formation of the titanium film has a barrier function of preventing diffusion of the conductive material. A copper film may be formed by a plating method after the formation of the barrier film of titanium, titanium nitride, or the like.

The wiring 156 can be formed in such a manner that a conductive layer is formed in contact with the source or drain electrode 154 and then etched selectively. The conductive layer can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. The details are similar to those of the source or drain electrode 142a or the like.

Through the above steps, the semiconductor device including the transistor 160, the transistor 162, and the capacitor 164 is completed.

In the semiconductor device described in this embodiment, the transistor 162 and the capacitor 164 overlap with the transistor 160, the transistor 160 does not include a sidewall insulating layer, and the source or drain electrode 142a is formed directly on the gate electrode 110, for example; accordingly, high integration is possible. Further, the manufacturing process is simplified.

Further, in the semiconductor device described in this embodiment, an insulating layer including hydrogen and an

insulating layer in which hydrogen is sufficiently reduced are used as the interlayer insulating layer 125 and the interlayer insulating layer 126, respectively; thus, the characteristics of the transistor 160 and the transistor 162 are improved. Owing to the insulating layer 143a and the insulating layer 143b, so-called gate capacitance is reduced and thus the operation speed of the transistor 162 is increased.

The above features described in this embodiment make it possible to provide a semiconductor device having extremely excellent characteristics.

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

Embodiment 7

In this embodiment, the cases where the semiconductor device described in any of the above embodiments is applied to an electronic device will be described with reference to FIGS. 16A to 16F. In this embodiment, the case where the above-described semiconductor device is applied to an electronic device such as a computer, a mobile phone (also referred to as a cellular phone or a mobile telephone device), a portable information terminal (including a portable game machine, an audio reproducing device, and the like), a digital camera, a digital video camera, an electronic paper, or a television device (also referred to as a television or a television receiver).

FIG. 16A illustrates a laptop computer including a housing 701, a housing 702, a display portion 703, a keyboard 704, and the like. The semiconductor devices described in any of the above embodiments are provided in the housing 701 and the housing 702. Therefore, the laptop computer can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

FIG. 16B illustrates a portable information terminal (personal digital assistance (PDA)). A main body 711 is provided with a display portion 713, an external interface 715, operation buttons 714, and the like. Further, a stylus 712 for operating the portable information terminal or the like is also provided. The semiconductor device described in any of the above embodiments is provided in the main body 711. Therefore, the portable information terminal can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

FIG. 16C illustrates an electronic book reader mounting electronic paper. The electronic book reader has two housings of a housing 721 and a housing 723. The housing 721 and the housing 723 are provided with a display portion 725 and a display portion 727, respectively. The housing 721 and the housing 723 are connected by a hinge 737 and can be opened and closed with the hinge 737 as an axis. Further, the housing 721 is provided with a power switch 731, operation keys 733, a speaker 735, and the like. At least one of the housing 721 and the housing 723 is provided with the semiconductor device described in any of the above embodiments. Therefore, the electronic book reader can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

FIG. 16D illustrates a mobile phone including two housings of a housing 740 and a housing 741. Further, the housing 740 and the housing 741 in a state where they are developed as illustrated in FIG. 16D can shift by sliding so that one is lapped over the other; therefore, the size of the mobile phone can be reduced, which makes the mobile phone suitable for being carried. The housing 741 is provided with a display

panel 742, a speaker 743, a microphone 744, an operation key 745, a pointing device 746, a camera lens 747, an external connection terminal 748, and the like. The housing 740 is provided with a solar cell 749 that charges the mobile phone, an external memory slot 750, and the like. Further, an antenna is incorporated in the housing 741. At least one of the housing 740 and the housing 741 is provided with the semiconductor device described in any of the above embodiments. Therefore, the mobile phone can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

FIG. 16E illustrates a digital camera including a main body 761, a display portion 767, an eyepiece 763, an operation switch 764, a display portion 765, a battery 766, and the like. The semiconductor device described in any of the above embodiments is provided in the main body 761. Therefore, the digital camera can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

FIG. 16F is a television device including a housing 771, a display portion 773, a stand 775, and the like. The television device can be operated by a switch of the housing 771 or a remote controller 780. The semiconductor devices described in any of the above embodiments are provided for the housing 771 and the remote controller 780. Therefore, the television device can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

Thus, the semiconductor device according to any of the above embodiments is provided for the electronic devices described in this embodiment. Accordingly, electronic devices with low power consumption can be realized.

Example 1

The number of times a semiconductor device according to an embodiment of the disclosed invention can rewrite data was examined. In this example, the examination results will be described with reference to FIG. 17.

A semiconductor device used for the examination is the semiconductor device having the circuit configuration in FIG. 1A-1. Here, an oxide semiconductor was used for a transistor corresponding to the transistor 162, and a capacitor with a capacitance value of 0.33 pF was used as a capacitor corresponding to the capacitor 164.

The examination was performed by comparing the initial memory window width and the memory window width at the time after storing and writing of data were repeated predetermined times. Data was stored and written by applying 0 V or 5 V to a wiring corresponding to the third wiring in FIG. 1A-1 and applying 0 V or 5 V to a wiring corresponding to the fourth wiring in FIG. 1A-1. When the potential of the wiring corresponding to the fourth wiring is 0 V, the transistor (writing transistor) corresponding to the transistor 162 is off; thus, a potential supplied to a node FG is held. When the potential of the wiring corresponding to the fourth wiring is 5 V, the transistor corresponding to the transistor 162 is on; thus, a potential of the wiring corresponding to the third wiring is supplied to the node FG.

The memory window width is one of indicators of the characteristics of a storage device. Here, the memory window width represents the shift amount $\Delta V_{cg}$ in curves ($V_{cg}$-$I_d$ curves) between different memory states, which show the relation between the potential $V_{cg}$ of a wiring corresponding to the fifth wiring and drain current $I_d$ of a transistor (reading transistor) corresponding to the transistor 160. The different memory states mean a state where 0 V is applied to a node FG

(hereinafter referred to as a Low state) and a state where 5 V is applied to a node FG (hereinafter referred to as a High state). That is, the memory window width can be checked by sweeping the potential $V_{cg}$ in the Low state and in the High state.

FIG. 17 shows the examination results of the initial memory window width and the memory window width at the time after writing was performed $1\times10^9$ times. Note that in FIG. 17, the horizontal axis shows $V_{cg}$ (V) and the vertical axis shows $I_d$ (A). According to FIG. 17, the memory window width is not changed after data is written $1\times10^9$ times, which means that the semiconductor device does not deteriorate at least during this period.

As described above, in a semiconductor device according to an embodiment of the disclosed invention, characteristics were not changed even after data was stored and written $1\times10^9$ times and resistance against rewriting was very high. That is, it can be said that according to an embodiment of the disclosed invention, a significantly reliable semiconductor device can be realized.

### Example 2

In this example, results obtained by measuring the off-state current of a transistor including a purified oxide semiconductor will be described.

In this example, a transistor including a purified oxide semiconductor was formed in accordance with Embodiment 4. First, a transistor with a channel width W of 1 m, which was sufficiently wide, was prepared in consideration of the very small off-state current of a transistor including a purified oxide semiconductor, and the off-state current was measured. FIG. 18 shows the results obtained by measurement of the off-state current of the transistor with a channel width W of 1 m. In FIG. 18, the horizontal axis shows gate voltage $V_G$ and the vertical axis shows drain current $I_D$. In the case where the drain voltage $V_D$ is +1 V or +10 V and the gate voltage $V_G$ is within the range of −5 V to −20 V, the off-state current of the thin film transistor was found to be less than or equal to $1\times10^{-13}$ A which is the detection limit. Moreover, it was found that the off current density of the transistor is lower than or equal to 1 aA/μm ($1\times10^{-18}$ A/μm).

Next will be described the results obtained by measuring the off-state current of the thin film transistor including a purified oxide semiconductor more accurately. As described above, the off-state current of the transistor including a purified oxide semiconductor was found to be less than or equal to $1\times10^{-13}$ A which is the detection limit of measurement equipment. Here, the results obtained by measuring more accurate off-state current (the value less than or equal to the detection limit of measurement equipment in the above measurement), with the use of an element for characteristic evaluation, will be described.

First, the element for characteristic evaluation which was used in a method for measuring current will be described with reference to FIG. 19.

In the element for characteristic evaluation in FIG. 19, three measurement systems 800 are connected in parallel. The measurement system 800 includes a capacitor 802, a transistor 804, a transistor 805, a transistor 806, and a transistor 808. A transistor manufactured in accordance with Embodiment 4 was used as each of the transistors 804 and 808.

In the measurement system 800, one of a source terminal and a drain terminal of the transistor 804, one terminal of the capacitor 802, and one of a source terminal and a drain terminal of the transistor 805 are connected to a power source

(for supplying $V_2$). The other of the source terminal and the drain terminal of the transistor 804, one of a source terminal and a drain terminal of the transistor 808, the other terminal of the capacitor 802, and a gate terminal of the transistor 805 are connected to one another. The other of the source terminal and the drain terminal of the transistor 808, one of a source terminal and a drain terminal of the transistor 806, and a gate terminal of the transistor 806 are connected to a power source (for supplying $V_1$). The other of the source terminal and the drain terminal of the transistor 805 and the other of the source terminal and the drain terminal of the transistor 806 are each electrically connected to an output terminal of $V_{out}$.

A potential $V_{ext\_b2}$ for controlling an on state and an off state of the transistor 804 is supplied to a gate terminal of the transistor 804. A potential $V_{ext\_b1}$ for controlling an on state and an off state of the transistor 808 is supplied to a gate terminal of the transistor 808. The potential $V_{out}$ is output from the output terminal.

Next, a method for measuring current with the use of the measurement system will be described.

First, an initialization period in which a potential difference is applied to measure the off-state current will be described briefly. In the initialization period, the potential $V_{ext\_b1}$ for turning on the transistor 808 is input to the gate terminal of the transistor 808, and the potential $V_1$ is supplied to a node A that is a node connected to the other of the source terminal and the drain terminal of the transistor 804 (that is, the node connected to one of the source terminal and the drain terminal of the transistor 808, the other terminal of the capacitor 802, and the gate terminal of the transistor 805). Here, the potential $V_1$ is, for example, a high potential. The transistor 804 is off.

After that, the potential $V_{ext\_b1}$ for turning off the transistor 808 is input to the gate terminal of the transistor 808, so that the transistor 808 is turned off. After the transistor 808 is turned off, the potential $V_1$ is set to low. The transistor 804 is still off. The potential $V_2$ is the same potential as the potential $V_1$. Thus, the initialization period is completed. In a state where the initialization period is completed, a potential difference is generated between the node A and one of the source terminal and the drain terminal of the transistor 804, and a potential difference is also generated between the node A and the other of the source terminal and the drain terminal of the transistor 808. Therefore, electric charge flows slightly through the transistor 804 and the transistor 808. In other words, off-state current is generated.

Next, a measurement period of the off-state current will be described briefly. In the measurement period, the potential of one of the source terminal and the drain terminal of the transistor 804 (that is, the potential $V_2$) and the potential of the other of the source terminal and the drain terminal of the transistor 808 (that is, the potential $V_1$) are set to low and fixed. On the other hand, the potential of the node A is not fixed (the node A is in a floating state) in the measurement period. Accordingly, electric charge flows through the transistor 804 and the amount of electric charge held at the node A is changed as time goes by. Further, as the amount of electric charge held at the node A is changed, the potential of the node A varies. That is to say, the output potential $V_{out}$ of the output terminal also varies.

FIG. 20 shows details (timing chart) of the relation between potentials in the initialization period in which the potential difference is generated and in the following measurement period.

In the initialization period, first, the potential $V_{ext\_b2}$ is set to a potential (high potential) at which the transistor 804 is turned on. Thus, the potential of the node A comes to be $V_2$,

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that is, a low potential ($V_{SS}$). After that, the potential $V_{ext\_b2}$ is set to a potential (low potential) at which the transistor **804** is turned off, whereby the transistor **804** is turned off. Then, the potential $V_{ext\_b1}$ is set to a potential (high potential) at which the transistor **808** is turned on. Thus, the potential of the node A comes to be $V_1$, that is, a high potential ($V_{DD}$). After that, the potential $V_{ext\_b1}$ is set to a potential at which the transistor **808** is turned off. Accordingly, the node A is brought into a floating state and the initialization period is completed.

In the following measurement period, the potential $V_1$ and the potential $V_2$ are individually set to potentials at which electric charge flows to or from the node A. Here, the potential $V_1$ and the potential $V_2$ are low potentials ($V_{SS}$). Note that at the timing of measuring the output potential $V_{out}$, it is necessary to operate an output circuit; thus, $V_1$ is set to a high potential ($V_{DD}$) temporarily in some cases. The period in which $V_1$ is a high potential ($V_{DD}$) is set to be short so that the measurement is not influenced.

When a potential difference is generated in the above-described manner to start the measurement period, the amount of electric charge held at the node A is changed as time goes by and accordingly, the potential of the node A varies. This means that the potential of the gate terminal of the transistor **805** varies and thus, the output potential $V_{out}$ of the output terminal also varies with the lapse of time.

A method for calculating the off-state current on the basis of the obtained output potential $V_{out}$ will be described below.

The relation between the potential $V_A$ of the node A and the output potential $V_{out}$ is obtained in advance before the off-state current is calculated. Thus, the potential $V_A$ of the node A can be obtained on the basis of the output potential $V_{out}$. From the relation described above, the potential $V_A$ of the node A can be expressed by the following equation as a function of the output potential $V_{out}$.

$$V_A = F(Vout) \qquad \text{[Equation 1]}$$

Electric charge $Q_A$ of the node A is expressed by the following equation, using the potential $V_A$ of the node A, capacitance $C_A$ connected to the node A, and a constant (const). Here, the capacitance $C_A$ connected to the node A is the sum of capacitance of the capacitor **802** and the other capacitance.

$$Q_A = C_A V_A + \text{const} \qquad \text{[Equation 2]}$$

Since current $I_A$ of the node A is obtained by differentiating electric charge flowing to the node A (or electric charge flowing from the node A) with respect to time, the current $I_A$ of the node A is expressed by the following equation.

$$I_A \equiv \frac{\Delta Q_A}{\Delta t} = \frac{C_A \Delta F(Vout)}{\Delta t} \qquad \text{[Equation 3]}$$

Thus, the current $I_A$ of the node A can be obtained on the basis of the capacitance $C_A$ connected to the node A and the output potential $V_{out}$ of the output terminal.

By the method described above, leakage current (off-state current) flowing between the source and the drain of the transistor which is off can be calculated.

In this example, the transistor **804** and the transistor **808** were manufactured using a purified oxide semiconductor. The ratio of the channel length (L) to the channel width (W) of the transistors was L/W=1⁄5. In the measurement systems **800** arranged in parallel, respective capacitance values of capacitors **802** were 100 fF, 1 pF, and 3 pF.

Note that the measurement according to this example was performed assuming that $V_{DD}$=5 V and $V_{SS}$=0 V are satisfied.

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In the measurement period, the potential $V_1$ was basically set to $V_{SS}$ and set to $V_{DD}$ only in a period of 100 msec every 10 seconds to 300 seconds, and $V_{out}$ was measured. Further, $\Delta t$ used in calculation of the current I flowing through an element was approximately 30,000 seconds.

FIG. **21** shows the relation between the output potential $V_{out}$ and elapsed time Time in the current measurement. According to FIG. **21**, the potential varies as time passes.

FIG. **22** shows the off-state current calculated on the basis of the above current measurement. Note that FIG. **22** shows the relation between source-drain voltage V and off-state current I. According to FIG. **22**, the off-state current was approximately 40 zA/μm under the condition that the source-drain voltage was 4 V. When the source-drain voltage was 3.1 V, the off-state current was less than or equal to 10 zA/μm. Note that 1 zA is equivalent to $10^{-21}$ A.

According to this example, it was confirmed that the off-state current was sufficiently small in a transistor including a purified oxide semiconductor.

This application is based on Japanese Patent Application serial no. 2009-298891 filed with Japan Patent Office on Dec. 28, 2009, Japanese Patent Application serial no. 2010-007488 filed with Japan Patent Office on Jan. 15, 2010, and Japanese Patent Application serial no. 2010-160954 filed with Japan Patent Office on Jul. 15, 2010 the entire contents of which are hereby incorporated by reference.

The invention claimed is:

1. A semiconductor device comprising:
   a first transistor comprising a gate electrode;
   a first insulating layer comprising an opening, wherein the gate electrode of the first transistor is positioned in the opening;
   a second transistor comprising:
   an oxide semiconductor layer on the first insulating layer;
   a first conductive layer and a second conductive layer over the oxide semiconductor layer;
   a second insulating layer over the oxide semiconductor layer, the first conductive layer, and the second conductive layer; and
   a gate electrode over the second insulating layer and overlapping with the oxide semiconductor layer,
   wherein the oxide semiconductor layer comprises indium and zinc, and
   wherein the first conductive layer is in contact with the surface of the gate electrode of the first transistor and the first insulating layer.

2. The semiconductor device according to claim **1**, wherein the oxide semiconductor layer further comprises gallium.

3. The semiconductor device according to claim **1**, wherein the first insulating layer is a silicon oxide film or a silicon oxynitride film.

4. The semiconductor device according to claim **1**, wherein the surface of the first insulating layer and the surface of the gate electrode of the first transistor are planarized by a chemical mechanical polishing.

5. The semiconductor device according to claim **1**, wherein the first conductive layer and the second conductive layer are each in contact with the oxide semiconductor layer.

6. The semiconductor device according to claim **1**, wherein the gate electrode of the second transistor overlaps with the first conductive layer and the second conductive layer.

7. The semiconductor device according to claim **1**, further comprising a third conductive layer over the second insulating layer, wherein the third conductive layer overlaps with the first conductive layer.

**8**. The semiconductor device according to claim **1**, wherein a channel formation region of the first transistor comprises a semiconductor material other than an oxide semiconductor material.

**9**. The semiconductor device according to claim **1**, wherein a channel formation region of the first transistor comprises silicon.

**10**. The semiconductor device according to claim **1**, wherein a channel formation region of the first transistor is located in a semiconductor substrate.

**11**. The semiconductor device according to claim **1**, wherein the oxide semiconductor layer comprises hydrogen in a concentration of $5\times10^{19}$ atoms/cm$^3$ or less.

**12**. A semiconductor device comprising:
a first transistor comprising a gate electrode;
a first insulating layer surrounding the gate electrode of the first transistor;
a second transistor comprising:
an oxide semiconductor layer on the first insulating layer;
a first conductive layer and a second conductive layer over the oxide semiconductor layer;
a second insulating layer over the oxide semiconductor layer, the first conductive layer, and the second conductive layer; and
a gate electrode over the second insulating layer and overlapping with the oxide semiconductor layer,
wherein the oxide semiconductor layer comprises indium and zinc,
wherein a surface of the gate electrode of the first transistor and a surface of the first insulating layer are included in a same planarized surface, and
wherein the first conductive layer is in contact with the surface of the gate electrode of the first transistor.

**13**. The semiconductor device according to claim **12**, wherein the oxide semiconductor layer further comprises gallium.

**14**. The semiconductor device according to claim **12**, wherein the first insulating layer is a silicon oxide film or a silicon oxynitride film.

**15**. The semiconductor device according to claim **12**, wherein the surface of the first insulating layer and the surface of the gate electrode of the first transistor are planarized by a chemical mechanical polishing.

**16**. The semiconductor device according to claim **12**, wherein the first conductive layer and the second conductive layer are each in contact with the oxide semiconductor layer.

**17**. The semiconductor device according to claim **12**, wherein the gate electrode of the second transistor overlaps with the first conductive layer and the second conductive layer.

**18**. The semiconductor device according to claim **12**, further comprising a third conductive layer over the second insulating layer, wherein the third conductive layer overlaps with the first conductive layer.

**19**. The semiconductor device according to claim **12**, wherein a channel formation region of the first transistor comprises a semiconductor material other than an oxide semiconductor material.

**20**. The semiconductor device according to claim **12**, wherein a channel formation region of the first transistor comprises silicon.

**21**. The semiconductor device according to claim **12**, wherein a channel formation region of the first transistor is located in a semiconductor substrate.

**22**. The semiconductor device according to claim **12**, wherein the oxide semiconductor layer comprises hydrogen in a concentration of $5\times10^{19}$ atoms/cm$^3$ or less.

**23**. A semiconductor device comprising:
a first transistor comprising a gate electrode;
a first insulating layer over the first transistor, wherein the gate electrode of the first transistor is exposed from the first insulating layer;
a second transistor comprising:
an oxide semiconductor layer on the first insulating layer;
a first conductive layer and a second conductive layer over the oxide semiconductor layer;
a second insulating layer over the oxide semiconductor layer, the first conductive layer, and the second conductive layer; and
a gate electrode over the second insulating layer and overlapping with the oxide semiconductor layer,
wherein the oxide semiconductor layer comprises indium and zinc, and
wherein the first conductive layer is in contact with the surface of the gate electrode of the first transistor and the first insulating layer.

**24**. The semiconductor device according to claim **23**, wherein the oxide semiconductor layer further comprises gallium.

**25**. The semiconductor device according to claim **23**, wherein the first insulating layer is a silicon oxide film or a silicon oxynitride film.

**26**. The semiconductor device according to claim **23**, wherein the surface of the first insulating layer and the surface of the gate electrode of the first transistor are planarized by a chemical mechanical polishing.

**27**. The semiconductor device according to claim **23**, wherein the first conductive layer and the second conductive layer are each in contact with the oxide semiconductor layer.

**28**. The semiconductor device according to claim **23**, wherein the gate electrode of the second transistor overlaps with the first conductive layer and the second conductive layer.

**29**. The semiconductor device according to claim **23**, further comprising a third conductive layer over the second insulating layer, wherein the third conductive layer overlaps with the first conductive layer.

**30**. The semiconductor device according to claim **23**, wherein a channel formation region of the first transistor comprises a semiconductor material other than an oxide semiconductor material.

**31**. The semiconductor device according to claim **23**, wherein a channel formation region of the first transistor comprises silicon.

**32**. The semiconductor device according to claim **23**, wherein a channel formation region of the first transistor is located in a semiconductor substrate.

**33**. The semiconductor device according to claim **23**, wherein the oxide semiconductor layer comprises hydrogen in a concentration of $5\times10^{19}$ atoms/cm$^3$ or less.

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